

MUMBAI UNIVERSITY
ELECTRONICS DEVICES & CIRCUITS-II
Semester 4 - December 19 - Choice Based

Q.1 a) State biasing techniques of Enhancement Type MOSFET and explain any one technique in detail .

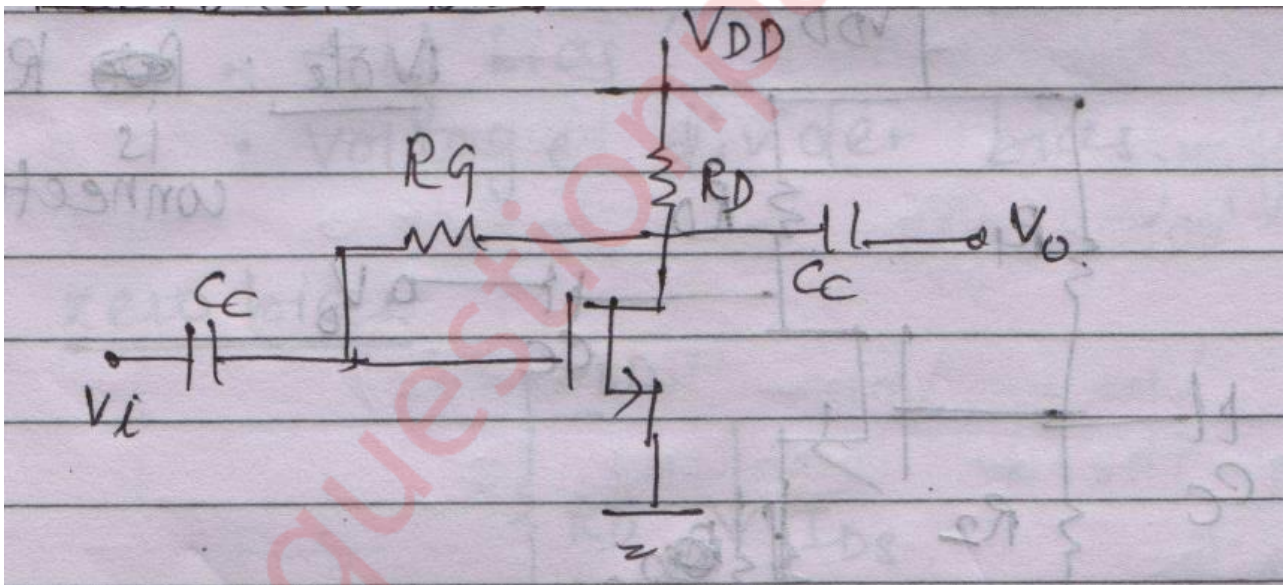
[5M]

Ans : i) Biasing techniques of Enhancement Type MOSFET :

--- Feedback Bias

--- Voltage Divider Bias

ii) Feedback Bias :



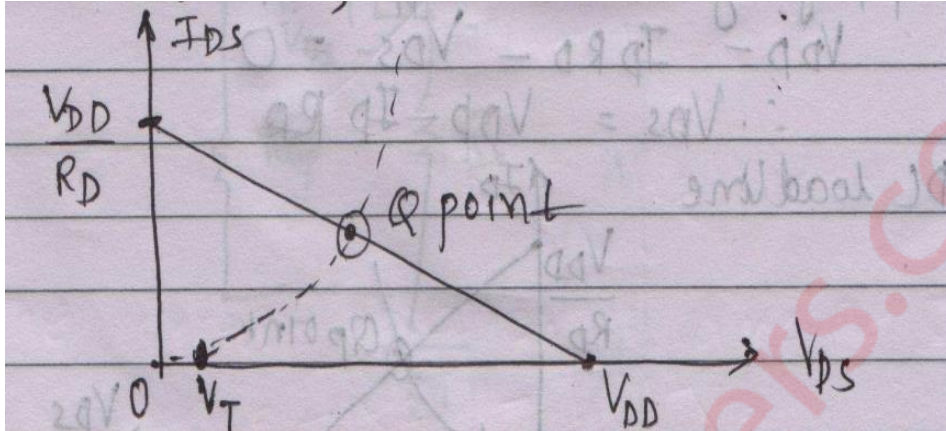
iii) The resistance R_g brings suitable high voltage to gate of MOSFET so as to drive it ON. Since drain to gate resistance R_g returns a part of output signal back to input, the circuit is called as feedback biasing circuit.

iv) Now we know that $V_{gs} = V_{ds}$ and using KVL,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D$$

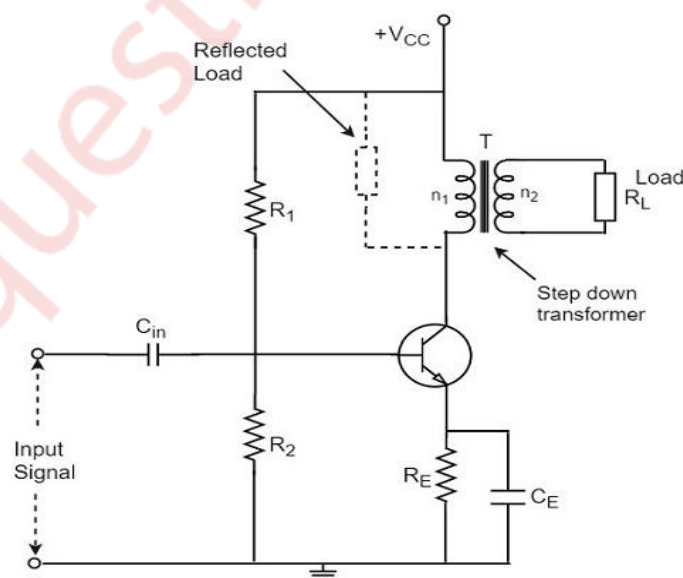
v) DC loadline is given by ,



b) Explain Transformer coupled amplifier and give its advantages and disadvantages. [5M]

Ans : i) When the collector current flows at all times during the full cycle of signal, the power amplifier is known as class A power amplifier. This is similar to the normal amplifier circuit but connected with a transformer in the collector load.

ii) Here R_1 and R_2 provide potential divider arrangement. The resistor R_e provides stabilization, C_e is the bypass capacitor and R_e to prevent a.c. voltage. The transformer used here is a step-down transformer.



iii) The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker).

iv) The transformer used in the collector circuit is for impedance matching. R_L is the load connected in the secondary of a transformer. R_L' is the reflected load in the primary of the transformer.

v) The number of turns in the primary are n_1 and the secondary are n_2 . Let V_1 and V_2 be the primary and secondary voltages and I_1 and I_2 be the primary and secondary currents respectively. The below figure shows the transformer clearly.

vi) If the peak value of the collector current due to signal is equal to zero signal collector current, then the maximum a.c. power output is obtained. So, in order to achieve complete amplification, the operating point should lie at the center of the load line.

vii) The operating point obviously varies when the signal is applied. The collector voltage varies in opposite phase to the collector current. The variation of collector voltage appears across the primary of the transformer.

viii) The efficiency of a class A power amplifier is nearly than 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

ix) Advantages :

The advantages of transformer coupled class A power amplifier are as follows. No loss of signal power in the base or collector resistors. Excellent impedance matching is achieved. Gain is high. DC isolation is provided.

x) Disadvantages

The disadvantages of transformer coupled class A power amplifier are as follows. Low frequency signals are less amplified comparatively. Hum noise is introduced by transformers. Transformers are bulky and costly. Poor frequency response.

xi) Applications

The applications of transformer coupled class A power amplifier are as follows. This circuit is where impedance matching is the main criterion. These are used as driver amplifiers and sometimes as output amplifiers.

c) Define efficiency for a power amplifier and write the expression for the same. State the efficiency of Class A , Class B and Class C Amplifier respectively. [5M]

Ans : i) When the DC supply is given by the battery but no AC signal input is given, the collector output at such a condition is observed as collector efficiency.

ii) The collector efficiency is defined as

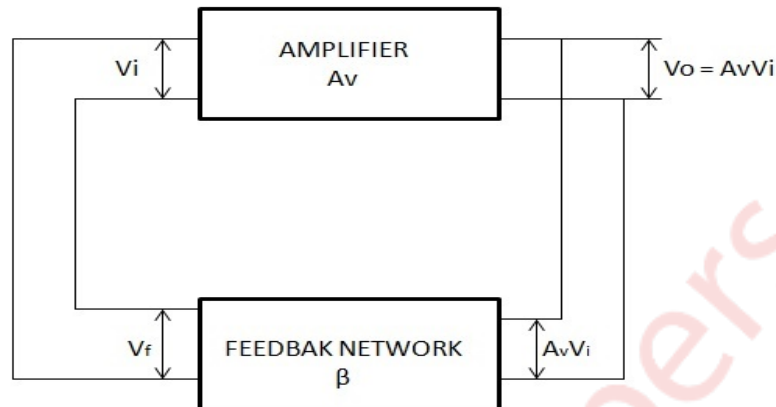
$$\eta = \frac{\text{Average A.C Power Output}}{\text{Average D.C power Input to transistor}}$$

	Class A Power Amp.	Class B Power Amp.	Class C Power Amp.
1.	In this amplifier , the operating point of BJT is at centre of loadline.	In this amplifier, operating point of BJT is in cut off region.	In this amplifier, operating point of BJT is below cut of region.
2.	Conduction angle lies in between 0 to 360 deg.	Conduction angle lies in between 0 to 180 deg.	Conduction angle lies in less than 90 deg.
3.	Overall efficiency of Class A power amplifier is poor. (25 % to 30 %)	Overall efficiency of Class B power amplifier is better. (70 % to 80 %)	Overall efficiency of Class C power amplifier is higher. (more than 80 %)
4.	Collector current flows at all times during full cycle of signal.	Collector current flows only during positive half cycle of input signal.	Collector current flows for less than half cycle of input signal.
5.	To achieve high linearity and gain, the output stage of a class A amplifier is biased "ON" (conducting) all the time	Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier	The Class C Amplifier design has the greatest efficiency but the poorest linearity of the classes of amplifiers
6.	As a class A amplifier operates in the linear portion of its characteristic curves, the single output device conducts through a full 360 degrees of the output waveform	In the class B amplifier, there is no DC base bias current as its quiescent current is zero, so that the dc power is small and therefore its efficiency is much higher than that of the class A amplifier	the output signals amplitude and phase are linearly related to the input signals amplitude and phase

d) Give the basic principle of an oscillator. State the types of Oscillators.

[5M]

Ans : i) An oscillator is an electronic circuit that generates sinusoidal oscillations known as sinusoidal oscillator. It converts input energy from a DC source into AC output energy of periodic waveform, at a specific frequency and is known amplitude. The characteristic feature of the oscillator is that it maintains its AC output.



ii) A sinusoidal oscillator is essentially a form of feedback amplifier, where special requirements are placed on the voltage gain A_v and the feedback networks β .

iii) The oscillator ckt works on barkhausen's criteria, which states that an amplifier can be converted into an oscillator provided that following conditions must be satisfied.

--- Amplifier must have positive f/b

--- The Total Phase shift of the loop or circuit must be 360° phase shift. The amplifier provides 180° phase shift and the feedback network provides another 180° phase shift. so the total phase shift of the circuit is 360° phase shift.

--- $|AB| \geq 1$ i.e. Loop gain value should be greater than or equal to one.

Q.2 a) Design a two stage RC coupled CS-CE Amplifier to meet following specifications:

$A_v \geq 750$, $S \leq 10$, $R_i \geq 1M\Omega$, $V_{cc} = 10V$.

Assume the following data : $\beta(\text{typ}) = 290$, $h_{ie} = 4.5K\Omega$, $g_{m0} = 5000\mu S$, $I_{DSS} = 7mA$,

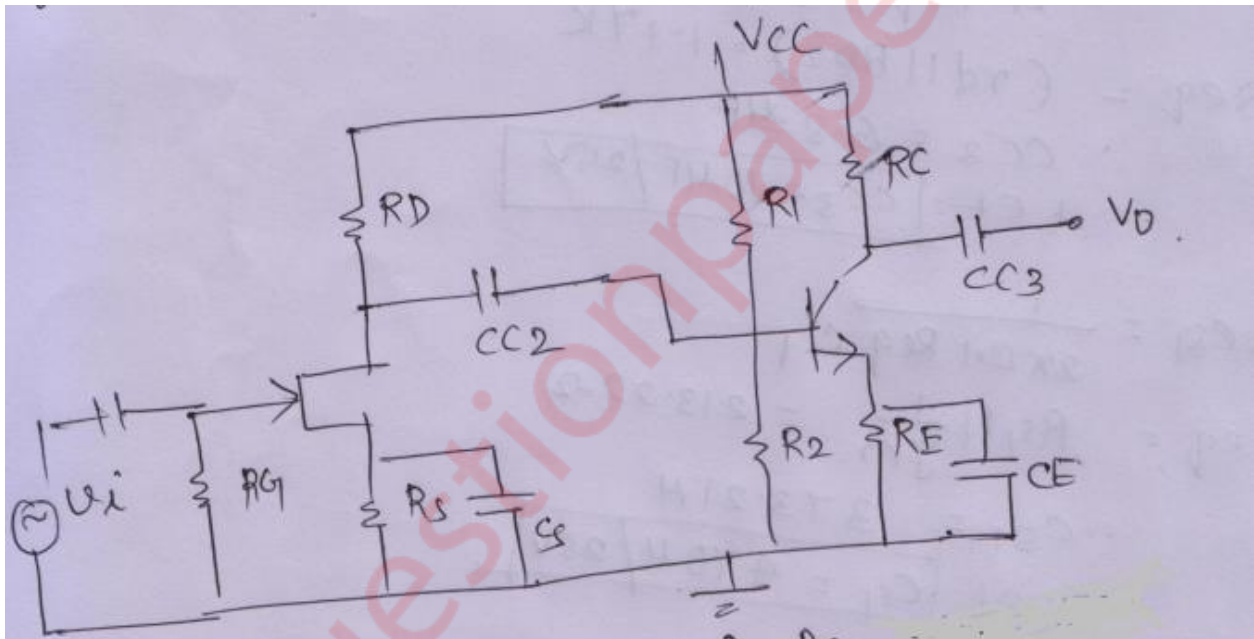
$r_d = 50K$, $V_p = -4V$.

[15M]

Ans : i) Given Specification : CS-CE Amplifier with gain of less than 500. Since input impedance is in $M\Omega$ first stage is common source JFET Amplifier and second stage is common emitter BJT amplifier. This both stages are RC coupled .

ii) Let the transistor used be BC 147B and BFW11.

iii) Circuit Diagram :



iv) Specifications of transistors :

A) BFW 11 :- $g_{m0} = 5000\mu S$, $I_{DSS} = 7mA$, $r_d = 50K$, $V_p = -4V$.

B) BC 147B :- $h_{ie} = 4.5K$, $V_{(CE\text{ sat})} = 0.25V$, $\beta(\text{typ}) = 290$

v) Let $A_v' = 5$ and $A_v'' = 150$ where A_v' = Gain of first stage and A_v'' = Gain of second stage. Here we know that ,

$$A_v'' = \frac{h_{fe(\text{min})} \cdot R_c}{h_{ie}} = \frac{240 \times R_c}{4.5K} = 2.87 K\Omega$$

Choosing HSV , $R_c = 3K \Omega / 0.25 W$

vi) Q-point : $V(CEQ) = V_{cc}/2 = 10/2 = 5 V$

Let $V(RE) = 10 \% \cdot V_{cc} = 0.1 V$

Applying KVL in input loop ,

$$V_{cc} - I_c \cdot R_c - V(CE) - V(RE) = 0$$

$$I(CQ) = 1.7 \text{ mA}$$

$$R_E = V(RE)/I_c = 0.1 / 1.7 = 0.05 K\Omega / 0.25 W$$

vii) Now lets find R_1 & R_2 using stability factor , $S = 10$

We know that , $S = 1 + \frac{R_{th}}{R_E} = 10 \Rightarrow R_{th} = 0.45 K\Omega$

Applying KVL in second stage input assuming thevenins equivalent circuit,

$$V_{th} - \frac{I_c}{h_{FE}} \cdot R_{th} - V(BE) - V(RE) = 0$$

$$V_{th} = 0.80 V$$

But we know that using thevenins rule ,

$$V_{th} = \frac{R_2}{R_1 + R_2} \cdot V_{cc} \quad \& \quad R_{th} = R_1 || R_2$$

On solving this , we will get , $R_1 = 6K\Omega / 0.25 W$ & $R_2 = 0.4K\Omega / 0.25 W$

viii) Now let us assume first stage , $A_v' = g_m \cdot (r_d || R_D || R_{th} || h_{ie})$

Considering midpoint biasing , $I(DS) = I(DSS)/2 = 3.5 \text{ mA}$

But , $I(DS) = I(DSS) \cdot [1 - \frac{V(GS)}{V_p}]^2$

$$3.5 \text{ m} = 7 \text{ m} \cdot [1 - \frac{V(GS)}{-4}]^2$$

$$V(GS) = -1.17 V$$

Now $g_m = g_{m0} [1 - \frac{V(GS)}{V_p}] \Rightarrow g_m = 3.53 \text{ m}\Omega$

Hence gain expression :

$$A_v' = g_m \cdot (r_d || R_D || R_{th} || h_{ie})$$

$$= (3.53 \text{ m}) \cdot (50K || R_D || 0.45K || 4.5K)$$

$$R_D = 0.6 K\Omega / 0.25 W$$

ix) Applying KVL in loop , $-V(GS) - I_D \cdot R_s = 0$

$$R_s = 330 \Omega / 0.25 W$$

x) To find capacitance used in circuits : Let us assume $f_L = 20 \text{ Hz}$

$$f_L(cc1) = \frac{1}{2\pi R_{eq} \cdot cc1} \Rightarrow R_{eq} = R_g = 1M \Omega \Rightarrow cc1 = 10 \text{ nF} / 25V$$

$$f_L(cc2) = \frac{1}{2\pi R_{eq} \cdot cc2} \Rightarrow R_{eq} = (r_d || R_d) + (R_{th} || h_{ie})$$

$$cc2 = 2.2 \text{ uF} / 25 \text{ V}$$

$$fL(cc3) = \frac{1}{2\pi Req.cc3} \Rightarrow Req = Rc = 2K \Omega$$

$$cc3 = 2.7 \text{ uF} / 25 \text{ V}$$

$$fL(cs) = \frac{1}{2\pi 0.1 Req.cs} \Rightarrow Req = Rs \parallel (1/gm)$$

$$cs = 690 \text{ uF} / 25 \text{ V}$$

$$fL(ce) = \frac{1}{2\pi 0.1 Req.ce} \Rightarrow Req = \frac{RD \parallel rd \parallel Rth + hie}{1 + hFE}$$

$$ce = 4.7 \text{ mf} / 25 \text{ V}$$

b) List various negative feedback topologies. Sketch any one topology.

[5M]

Ans : Various negative feedback topologies :

---Voltage Series Feedback Amplifier

---Voltage Shunt Feedback Amplifier

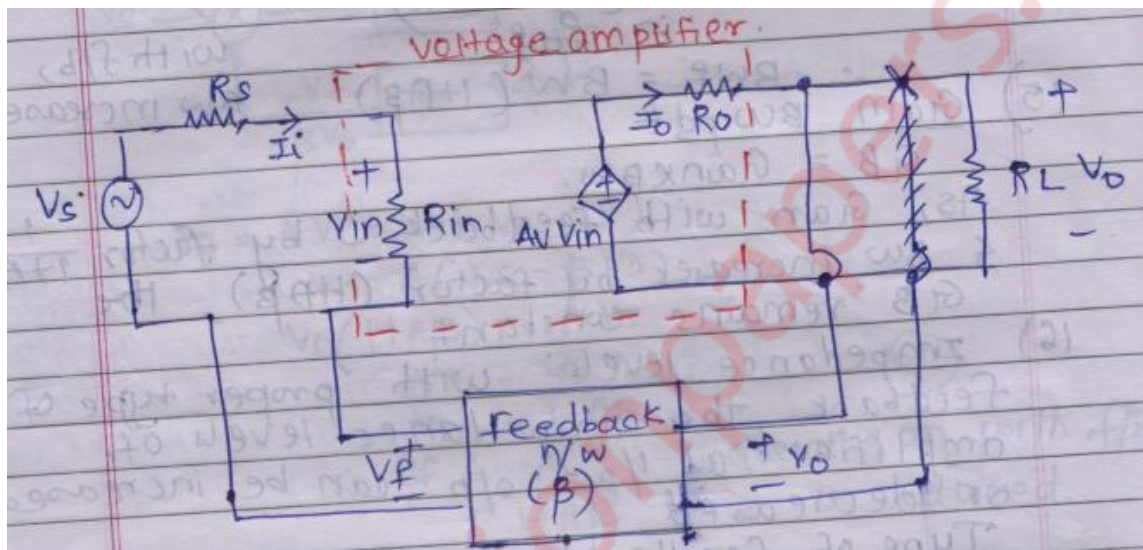
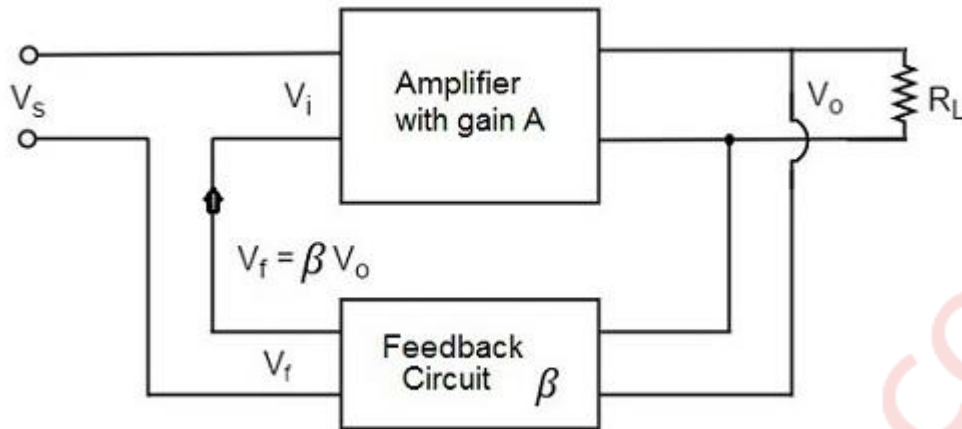
---Current Series Feedback Amplifier

---Current Shunt Feedback Amplifier

a) Voltage Series Feedback Amplifier

In this type of circuit, a portion of the o/p voltage can be applied to the input voltage in series through the feedback circuit. The block diagram of the voltage series feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output although in series by means of the input.

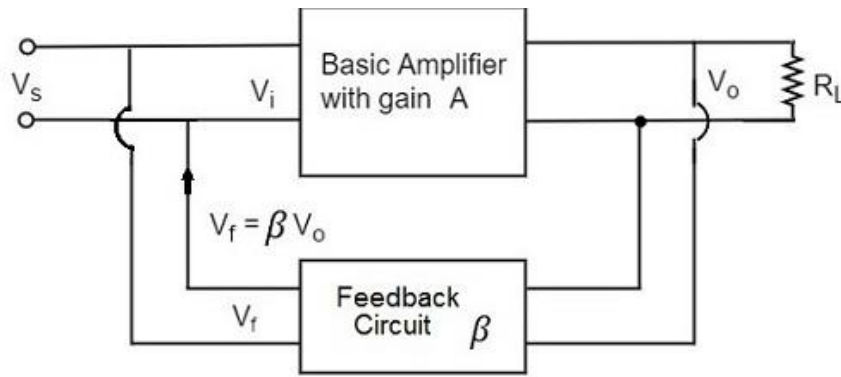
When the feedback circuit is allied in shunt through the output, then the o/p impedance will be reduced and the i/p impedance is enlarged because of the series connection with the input.



b) Voltage Shunt Feedback Amplifier

In this type of circuit, a portion of the o/p voltage can be applied to the input voltage in parallel with through the feedback circuit. The block diagram of the voltage shunt feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output as well as the input.

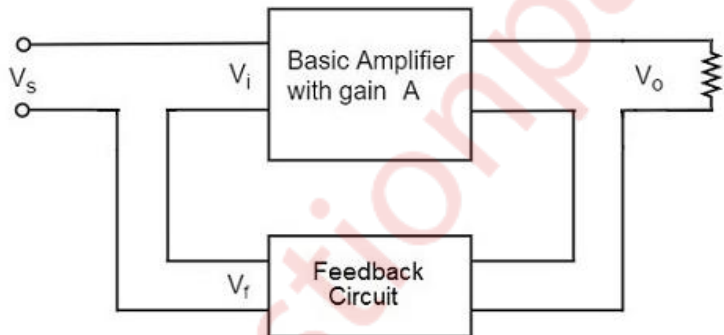
When the feedback circuit is allied in shunt through the o/p as well as the input, then both the o/p impedance & the i/p impedance will be decreased.



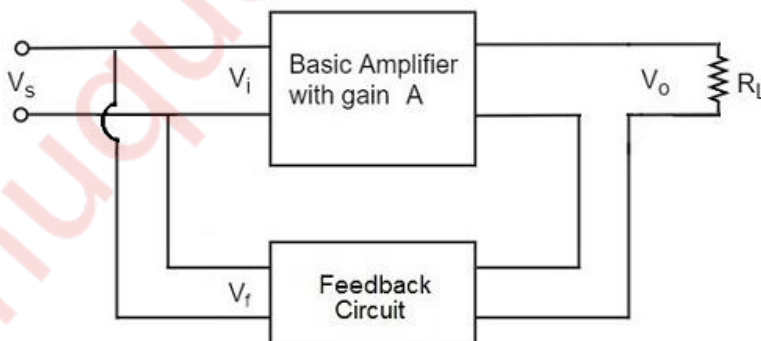
c) Current Series Feedback Amplifier

In this type of circuit, a portion of the o/p voltage is applied to the i/p voltage in series through the feedback circuit. The block diagram of the current series feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in series by means of the output as well as the input.

When the feedback circuit is allied in series through the o/p as well as the input, then both the o/p impedance & the i/p impedance will be increased.



d) Current Shunt Feedback Amplifier :

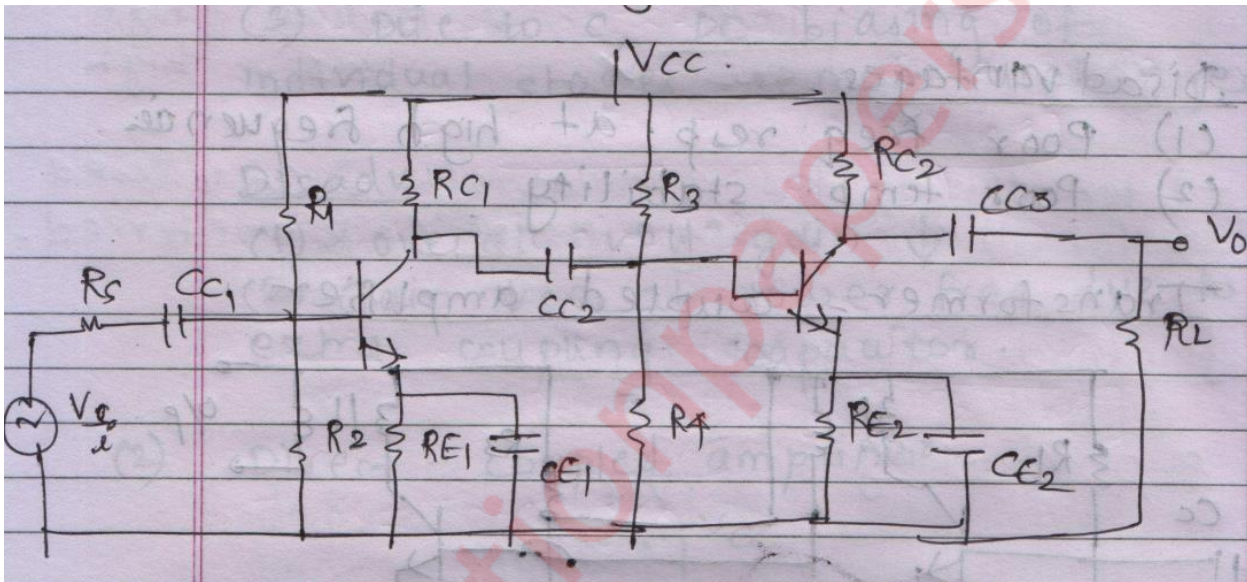


In this type of circuit, a portion of the o/p voltage is applied to the i/p voltage in shunt through the feedback circuit. The block diagram of the current shunt feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output as well as the input

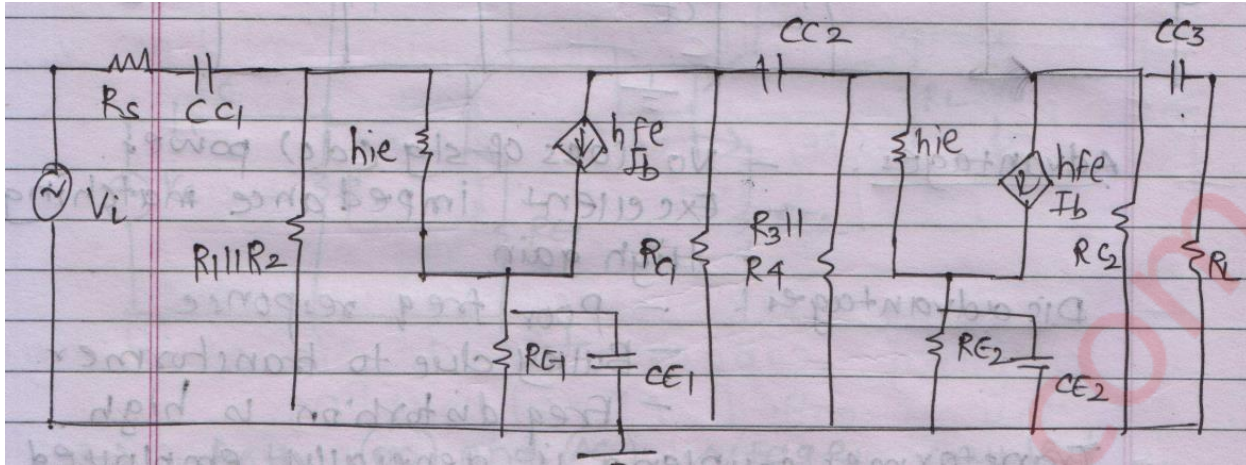
Q.3 a) Sketch circuit diagram , AC equivalent model and derive expression for input impedance ,output impedance , voltage gain and current gain of a two stage CE amplifier.

[10M]

Ans : i) Circuit Diagram of two stage CE amplifier :



ii) AC equivalent model of two stage CE-CE amplifier :



iii) Derivation For Voltage gain :

We know that voltage gain is given by , $A_v = \frac{V_o}{V_{in}} = \frac{V_o V_x}{V_x V_{in}}$

$$\frac{V_o}{V_x} = \frac{-hFE \cdot I_b (R_{c2} || RL)}{I_b \cdot hie} = \frac{-hFE (R_{c2} || RL)}{hie}$$

$$\frac{V_x}{V_i} = \frac{-hFE \cdot I_b (R_{c1} || R_3 || R_4 || hie)}{V_i}$$

$$\text{But , } I_b = \frac{(R_1 || R_2)}{(R_1 || R_2) + hie} \cdot I_i$$

$$V_i = I_i (R_s + z \cdot i_1)$$

where $z = (R_1 || R_2) + hie$

$$V_i = \frac{(R_s + Z_{11}) \cdot I_b \cdot [(R_1 || R_2) + hie]}{R_1 || R_2}$$

Substitute value of V_i ,

$$\frac{V_x}{V_i} = \frac{-hfe \cdot I_b ((R_{c1} || R_3 || R_4 || hie))}{(R_s + Z_{11}) \cdot I_b \cdot [(R_1 || R_2) + hie]} \cdot \frac{R_1 || R_2}{R_1 || R_2}$$

iv) For midband frequency model , short all coupling capacitors and bypass capacitors, input and output impedance is given by ,

$$Z_{in} = (R_1 || R_2) + hie$$

$$Z_o = R_c + RL$$

v) When an AC input signal is applied to the base of first transistor, it gets amplified and appears at the collector load R_L which is then passed through the coupling capacitor

CC to the next stage. This becomes the input of the next stage, whose amplified output again appears across its collector load. Thus the signal is amplified in stage by stage action.

vi) The important point that has to be noted here is that the total gain is less than the product of the gains of individual stages. This is because when a second stage is made to follow the first stage, the effective load resistance of the first stage is reduced due to the shunting effect of the input resistance of the second stage. Hence, in a multistage amplifier, only the gain of the last stage remains unchanged.

vii) As we consider a two stage amplifier here, the output phase is same as input. Because the phase reversal is done two times by the two stage CE configured amplifier circuit

viii) At Low frequencies (i.e. below 50 Hz)

The capacitive reactance is inversely proportional to the frequency. At low frequencies, the reactance is quite high. The reactance of input capacitor C_{in} and the coupling capacitor CC are so high that only small part of the input signal is allowed. The reactance of the emitter by pass capacitor CE is also very high during low frequencies. Hence it cannot shunt the emitter resistance effectively. With all these factors, the voltage gain rolls off at low frequencies.

ix) At High frequencies (i.e. above 20 KHz)

Again considering the same point, we know that the capacitive reactance is low at high frequencies. So, a capacitor behaves as a short circuit, at high frequencies. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. Along with this, as the capacitance of emitter diode decreases, it increases the base current of the transistor due to which the current gain (β) reduces. Hence the voltage gain rolls off at high frequencies.

x) At Mid-frequencies (i.e. 50 Hz to 20 KHz)

The voltage gain of the capacitors is maintained constant in this range of frequencies, as shown in figure. If the frequency increases, the reactance of the capacitor CC decreases which tends to increase the gain. But this lower capacitance reactive increases the loading effect of the next stage by which there is a reduction in gain. Due to these two factors, the gain is maintained constant

b) For 'n' stage cascaded amplifier, show that overall lower 3 dB cut-off frequency is

$$f_{LT} = \frac{f_L}{\sqrt{2^{1/n} - 1}} \text{ and overall higher frequency is } f_{H'} = f_H(\sqrt{2^{1/n} - 1}). \quad [10M]$$

Ans : We know that for 'n' stage cascaded amplifier,

$$\left(\frac{1}{\sqrt{1 + \left(\frac{fL}{fL(n)}\right)^2}} \right)^n = \frac{1}{\sqrt{2}}$$

$$\therefore \left(\sqrt{1 + \left(\frac{fL}{fL(n)}\right)^2} \right)^n = \sqrt{2}$$

Squaring on both sides and taking nth root,

$$\therefore 2^{1/n} = 1 + \left(\frac{fL}{fL(n)}\right)^2$$

$$\therefore 2^{1/n} - 1 = \left(\frac{fL}{fL(n)}\right)^2$$

Taking square root on both side,

$$\therefore \sqrt{2^{1/n} - 1} = \left(\frac{fL}{fL(n)}\right)$$

$$\therefore f_{LT} = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

Where, $f_L(n)$ = Lower 3dB frequency of identical cascaded stages.

f_L = Lower 3dB frequency of single stage

n = number of stages.

$$\left| \frac{\text{Overall } A_{V(\text{high})}}{\text{Overall } A_{V(\text{mid})}} \right| = \left[\frac{1}{\sqrt{1 + [f_H(n)/f_H]^2}} \right]^n = \frac{1}{\sqrt{2}}$$

$$\left[\sqrt{1 + [f_H(n)/f_H]^2} \right]^n = \sqrt{2}$$

Squaring both the sides,

$$[1 + [f_H(n)/f_H]^2]^n = 2^{1/n}$$

$$[f_H(n)/f_H]^2 = 2^{1/n} - 1$$

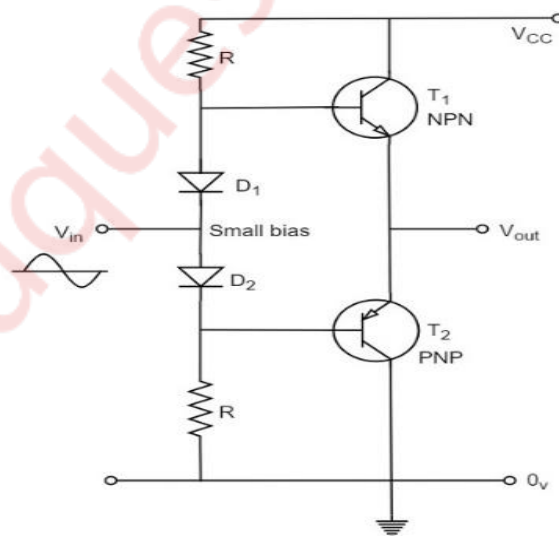
Taking square root of both the sides,

$$\frac{f_H(n)}{f_H} = \sqrt{2^{1/n} - 1}$$

$$f_H(n) = f_H \sqrt{2^{1/n} - 1}$$

Q.4 a) Draw a neat diagram of Class AB power amplifier and explain its working. [10M]

Ans : i) As the name implies, class AB is a combination of class A and class B type of amplifiers. As class A has the problem of low efficiency and class B has distortion problem, this class AB is emerged to eliminate these two problems, by utilizing the advantages of both the classes.

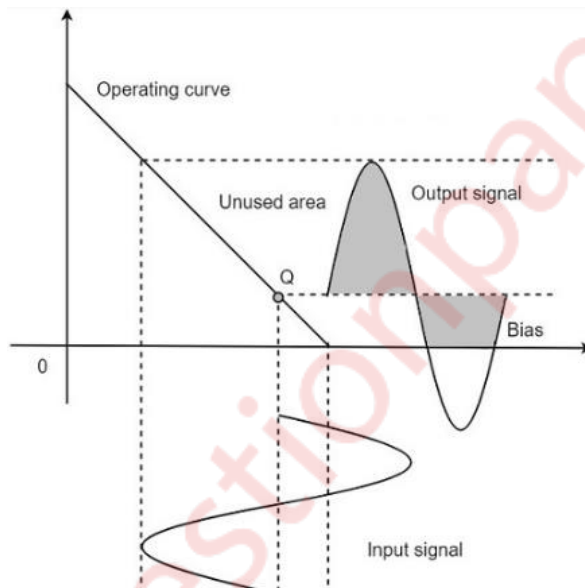


ii) The cross over distortion is the problem that occurs when both the transistors are OFF at the same instant, during the transition period. In order to eliminate this, the condition has to be chosen for more than one half cycle.

iii) Hence, the other transistor gets into conduction, before the operating transistor switches to cut off state. This is achieved only by using class AB configuration, as shown in the following circuit diagram.

iv) Therefore, in class AB amplifier design, each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A.

v) The conduction angle of class AB amplifier is somewhere between 180° to 360° depending upon the operating point selected. This is understood with the help of below figure



vi) The small bias voltage given using diodes D_1 and D_2 , as shown in the above figure, helps the operating point to be above the cutoff point. Hence the output waveform of class AB results as seen in the above figure.

vii) The crossover distortion created by class B is overcome by this class AB, as well the inefficiencies of class A and B don't affect the circuit.

viii) So, the class AB is a good compromise between class A and class B in terms of efficiency and linearity having the efficiency reaching about 50% to 60%. The class A, B and AB amplifiers are called as linear amplifiers because the output signal amplitude and phase are linearly related to the input signal amplitude and phase.

b) What is cascode amplifier ? Explain in detail.

[10M]

Ans : i) Cascode amplifier is the two stage amplifier in which common emitter stage is connected to common base stage. The input signal is applied at Q1 i.e at common emitter stage and output is obtained at Q2.

ii) A common-base configuration is not subject to the Miller effect because the grounded base shields the collector signal from being fed back to the emitter input. Thus, a C-B amplifier has better high frequency response. The way to reduce the common-emitter gain is to reduce the load resistance.

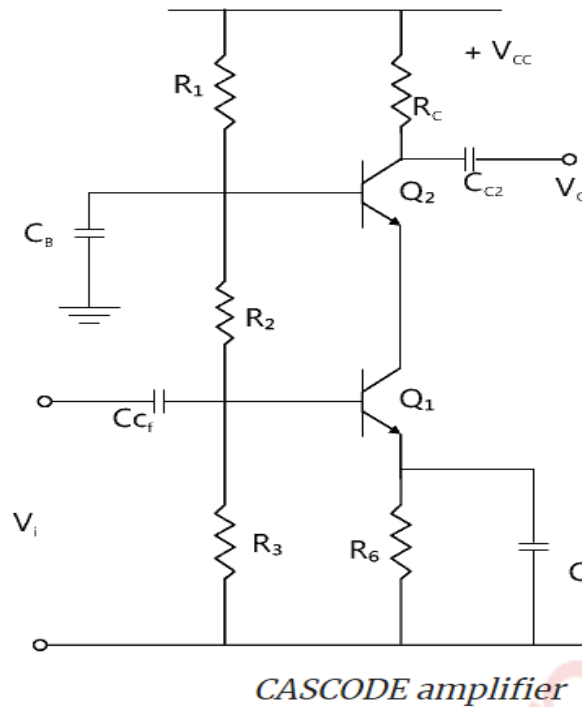
iii) The gain of a C-E amplifier is approximately R_c/R_e . The collector load R_c is the resistance of the emitter of the C-B stage loading the C-E stage. CE gain amplifier gain is approximately $A_v = R_c/R_e = 1$. This Miller capacitance is $C_{\text{Miller}} = C_{cbo}(1-A_v) = C_{cbo}(1-(-1)) = 2 C_{cbo}$. Cascode amplifier $15 C_{cbo}(1-(-1)) = 2 C_{cbo}$. We now have a moderately high input impedance C-E stage without suffering the Miller effect, but no C-E stage voltage gain. The C-B stage provides a high voltage gain.

iv) The total current gain of cascode is β as current gain of the C-E stage is 1 for the C-B is β . A cascode amplifier has a high gain, moderately high input impedance, a high output impedance, and a high bandwidth.

v) The cascode is a two-stage amplifier composed of a single transconductance amplifier (usually a common source/emitter stage) followed by a current follower (usually a common gate/base stage).

vi) Compared to a single amplifier stage, this combination may have one or more of the following advantages: higher input-output isolation, higher input impedance, higher output impedance, higher gain or higher bandwidth. In modern circuits, the cascode is often constructed from two transistors (BJTs or FETs), with one operating as a common emitter/source and the other as a common base/gate.

vii) The cascode improves input-output isolation (or reverse transmission) as there is less direct coupling from the output to input. This greatly reduces the Miller multiplication of stray coupling capacitance between input and output and thus contributes to a much higher bandwidth.



viii) The advantage of the cascode configuration stems from the placement of an upper transistor as the load of the input transistor's output terminal (collector / drain). This upper transistor is referred to as the cascode device. Because at high frequencies the cascode transistor's base/gate is effectively grounded by DC voltage source VBias, the cascode device's emitter / source voltage (and therefore the lower input transistor's collector / drain) is held at a more constant voltage during operation. In other words, the cascode device exhibits a low input resistance to the lower transistor, making the voltage gain seen at the collector / drain of the lower device very small, which dramatically reduces the Miller feedback capacitance from the lower transistor's collector to base or drain to gate.

ix) This loss of voltage gain is recovered by the cascode transistor. Thus, the cascode transistor permits the lower common emitter / source stage to operate with minimum negative (Miller) feedback, improving the bandwidth of the overall amplifier.

x) The base or gate of the cascode device is electrically AC grounded, so charge and discharge of stray capacitance C_{cb} or C_{dg} between collector and base or drain and gate is simply through R_L the output load, and the frequency response is affected only for frequencies above the associated RC time constant: In the case of a FET device $t = C_{dg} R_D || R_{out}$, a rather high frequency because C_{dg} is small. That is, the upper FET gate does not suffer from Miller multiplication of C_{dg} .

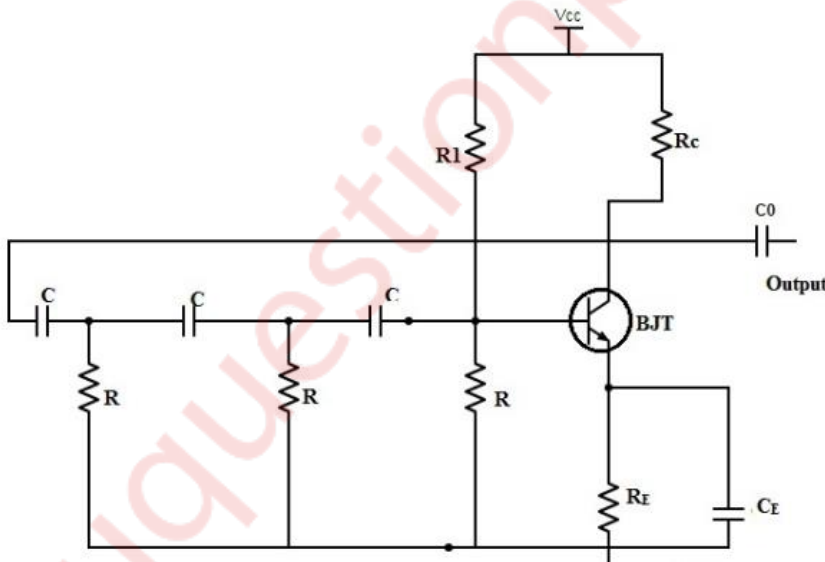
xi) If the cascode device stage were operated alone using its emitter or source as input node (i.e. common base/gate configuration), it would have good voltage gain and wide bandwidth. However, its low input impedance would limit its usefulness to very low impedance voltage drivers. Adding the lower common emitter/source stage results in an increased input impedance, allowing the cascode stage to be driven by a higher impedance source.

xii) If one were to replace the upper device with a typical resistive load, and take the output from the input transistor's collector or drain the common emitter/source configuration would offer the same input impedance as the cascode configuration, but the cascode configuration would offer a potentially greater gain and much greater bandwidth.

Q.5 a) Draw RC phase shift oscillator using BJT and derive the frequency of oscillation for same.

[10M]

Ans : i) The following RC phase shift oscillator circuit using BJT can be built by cascading 3-RC phase shift networks; each provides a 60deg. phase shift. In the circuit, the RC which is known as the collector resistor stops the transistor's collector current.



ii) The resistor which is near to the transistors like R & R1 can form the voltage divider circuit as the RE (emitter resistor) develops the strength. After that, the two capacitors namely Co & CE, where Co is the o/p DC decoupling capacitor & CE is the emitter bypass capacitor correspondingly. Further, this circuit also demonstrates 3-RC networks used within the feedback path.

iii) This connection will cause the o/p waveform to move with 180deg. throughout its journey from o/p terminal toward the transistor's base terminal.

iv) After that, this signal can be moved once more with 180deg. with the help of the transistor within the network because of the truth that the phase disparity among the input as well as the output can be 180 deg. in the common emitter (CE) configuration. This will create the network phase disparity to 360 degrees and satisfies the phase disparity condition.

v) Derivation for frequency of oscillations :

$$-I_1.Rc - \frac{1}{j.w.c}I_1 - (I_1 - I_2)R - hFE.I_b.Rc = 0$$

$$-I_1.Rc - \frac{1}{j.w.c}I_1 - (I_1).R + (I_2)R = hFE.Rc.I_b$$

$$(hFE.Rc.I_b + (I_2)R = I_1[Rc + \frac{1}{j.w.c} + R]) \quad \dots\dots\dots(1)$$

$$-(I_2 - I_1)R - \frac{1}{j.w.c}I_2 - (I_2 - I_3)R = 0$$

$$I_1.R - I_2 \left[2R + \frac{1}{j.w.c} \right] + I_3.R = 0 \quad \dots\dots\dots(2)$$

Similarly,

$$I_2.R - I_3 \left[2R + \frac{1}{j.w.c} \right] = 0 \quad \dots\dots\dots(3)$$

Let $\alpha = \frac{1}{w.Rc}$ and $k = \frac{Rc}{R}$

Get I1,I2 in terms of I3.

From equation 3 after dividing by R,

$$I_2 = I_3[2 - j.\alpha]$$

From equation 2 ,

$$I_1 = I_3[3j.4.\alpha - \alpha^2]$$

Substitute in equation 1,we will get ,

$$-hFE.k.I_b = I_3[1 + 3.k - (5 + k)\alpha^2 - j(6\alpha + 4\alpha k - \alpha^3)]$$

$$\text{Now, } \frac{I_3}{I_b} = \frac{-hFE.k}{[1 + 3.k - (5 + k)\alpha^2 - j(6\alpha + 4\alpha k - \alpha^3)]}$$

Loop gain is always real , $6\alpha + 4\alpha k - \alpha^3 = 0$

$$6 + 4k = \alpha^2$$

$$\alpha = \frac{1}{w.R.C}$$

Squaring we will get , $w^2 = \frac{1}{(6+4k)R^2C^2}$ but $w = 2\pi f$

Hence ,

$$f = \frac{1}{2\pi R.C.\sqrt{(6+4k)}}$$

$$\text{where } k = \frac{Rc}{R}$$

For sustained oscillations , $\frac{I_3}{I_b} > 1 \quad \therefore hFe > 4k + 23 + \frac{29}{k}$

vi) The advantages of this phase shift oscillator include the following :

---The oscillator circuit designing is easy with basic components like resistors as well as capacitors.

---This circuit is not expensive and gives excellent frequency stability.

---These are mainly suitable for low-frequencies

---This circuit is simpler compared with a Wein bridge oscillator because it doesn't require the stabilization planning & negative feedback.

---The circuit output is sinusoidal that is somewhat distortion free.

---The frequency range of this circuit will range from a few Hz to hundreds of kHz

vii) Disadvantages of RC-Phase Shift Oscillator : -

---The disadvantages of this phase shift oscillator include the following.

---The output of this circuit is small because of the smaller feedback

---It requires 12 volts battery for developing a suitably huge feedback voltage.

---It is hard for this circuit to create oscillations because of the small feedback

---The frequency stability of this circuit is not good to compare with Wien bridge oscillator.

viii) RC Phase Shift Oscillator Applications :-

---The applications of this type of phase shift oscillator include the following

---This phase shift oscillator is used to generate the signals over an extensive range of frequency. They used in musical instruments, GPS units, & voice synthesis.

---The applications of this phase shift oscillator include voice synthesis, musical instruments, and GPS units.

b) Enumerate the effects of negative feedback on Gain,Bandwidth,Distortion,input and output impedance .

[10M]

Ans : i) Feedback is the process by which a fraction of the output signal, either a voltage or a current, is used as an input. If this feed back fraction is opposite in value or phase (“anti-phase”) to the input signal, then the feedback is said to be Negative Feedback, or degenerative feedback.

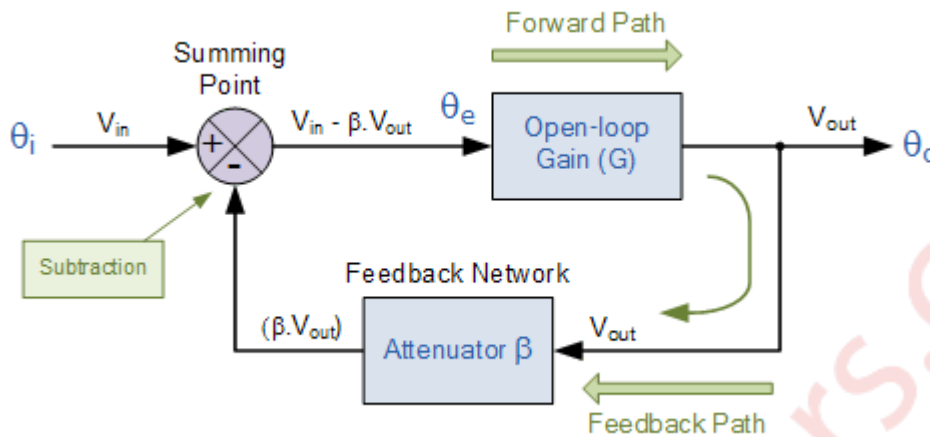
ii) Negative feedback opposes or subtracts from the input signals giving it many advantages in the design and stabilisation of control systems. For example, if the systems output changes for any reason, then negative feedback affects the input in such a way as to counteract the change.

iii) Feedback reduces the overall gain of a system with the degree of reduction being related to the systems open-loop gain. Negative feedback also has effects of reducing distortion, noise, sensitivity to external changes as well as improving system bandwidth and input and output impedances.

iv) Feedback in an electronic system, whether negative feedback or positive feedback is unilateral in direction. Meaning that its signals flow one way only from the output to the input of the system. This then makes the loop gain, G of the system independent of the load and source impedances.

v) As feedback implies a closed-loop system it must therefore have a summing point. In a negative feedback system this summing point or junction at its input subtracts the feedback signal from the input signal to form an error signal, β which drives the system.

If the system has a positive gain, the feedback signal must be subtracted from the input signal in order for the feedback to be negative as shown.



vi) The circuit represents a system with positive gain, G and feedback, β . The summing junction at its input subtracts the feedback signal from the input signal to form the error signal $V_{in} - \beta G$, which drives the system.

vii) Then using the basic closed-loop circuit above we can derive the general feedback equation as being:

viii) Negative Feedback Equation

System Gain = $G = V_{out}/V_{in}$ G is open loop gain

$G \cdot V_{in} = V_{out}$

$G(V_{in} - \beta \cdot V_{out}) = V_{out}$ where β = feedback fraction

$G_v = G/(1 + \beta G)$ Where G_v = closed loop gain

ix) We see that the effect of the negative feedback is to reduce the gain by the factor of: $1 + \beta G$. This factor is called the “feedback factor” or “amount of feedback” and is often specified in decibels (dB) by the relationship of $20 \log (1 + \beta G)$.

x) Effects of Negative Feedback

If the open-loop gain, G is very large, then βG will be much greater than 1, so that the overall gain of the system is roughly equal to $1/\beta$. If the open-loop gain decreases due to

frequency or the effects of system ageing, providing that βG is still relatively large, the overall system gain does not change very much. So negative feedback tends to reduce the effects of gain change giving what is generally called “gain stability”.

Feedback Topology	Input Resistance	Output Resistance
Voltage Series	Increases $R_{if} = R_i(1+A*\beta)$	Decreases $R_{of} = R_o/(1+A*\beta)$
Current Series	Increases $R_{if} = R_i(1+A*\beta)$	Increases $R_{of} = R_o(1+A*\beta)$
Current Shunt	Decreases $R_{if} = R_i/(1+A*\beta)$	Increases $R_{of} = R_o(1+A*\beta)$
Voltage Shunt	Decreases $R_{if} = R_i(1+A*\beta)$	Decreases $R_{of} = R_o/(1+A*\beta)$

Q.6 a) Compare small signal and large signal amplifier.

[5M]

Ans :

No.	Small Signal Amplifiers	Large Signal Amplifiers
1.	When the input signal is so weak so as to produce small fluctuations in the collector current compared to its quiescent value, the amplifier is known as Small signal amplifier.	When the fluctuations in collector current are large i.e. beyond the linear portion of the characteristics, the amplifier is known as large signal amplifier
2.	In small signal amplifiers main factors are usually amplification linearity and magnitude of gain.	In large signal amplifiers main facto is power efficiency of amplifiers.
3.	Since current and voltage are small , power handling capacity of this amplifiers are less and little concern.	Since large signals are at input and producing large amount of current in many conditions results into high power handling capacity.
4.	Impedance matching at output is not major concern.	Impedance matching is one of the most important factor in large asignal amplifiers.
5.	Small signal models are used to determine how the output responds to input signal.	Large signal models are used to determine the DC operating point of BJT.
6.	Main factors are : 1.Amplification 2.Linearity 3. Gain	Main factors are : 1. Efficiency 2.Maximum power capability 3. Impedance matching to output devices.

b) Calculate frequency of oscillation for Hartley oscillator if $L_1=5\text{mH}$, $L_2=2\text{mH}$ and $C=0.2\ \mu\text{F}$.

[5M]

Ans : Given : $L_1 = 5\text{mH}$, $L_2 = 2\text{mH}$, $C = 0.2\ \mu\text{F}$

To Find : Frequency of oscillations for hatley oscillator = $f = ?$

Formula : $f_r = \frac{1}{2\pi\sqrt{L.C}}$ $L = L1 + L2$

Solution : We know that the frequency of oscillations for Hartley oscillator is ,

$$f = \frac{1}{2\pi\sqrt{(L1+L2).C}}$$

$$\therefore f = \frac{1}{2\pi\sqrt{(5m + 2m).(0.2\mu)}}$$

$$\therefore f = 4.25 \text{ KHz}$$

c) Explain the concept of Heat sink in detail required for power amplifiers.

[5M]

Ans : i) Heat sinks are used for power transistors as the power dissipated at their collector junction is large. If heat dissipation is not done, this will cause large increases in junction temperature. In a transistor, the collector to base junction temperature (temperature of surrounding air) rises or because of self-heating.

ii) The self-heating is due to the power dissipated at collector junction. This power dissipation at junction causes the junction temperature to rise, and this in turn increases the collector current which causes further increase in power dissipation. If the phenomenon continues then it may result in permanent damage of the transistor. This is known as thermal runaway.

iii) In power transistor or large signal transistors, the power to be dissipated at the collector causes junction temperature to rise to a high level. It is possible to increase the power handling capacity of the transistor if a device that can cause rapid conduction of heat away from the junction is used. Such a device is called a heat sink. A heat sink is a mechanical device. It is connected to the case of the semiconductor device. So it is providing a path for the heat transfer. The heat flows through the heat sink and is radiated to surrounding air. If a heat sink is not used then all the heat has to be transferred from a transistor case to surrounding air causing case temperature to increase. If the power handled by the transistor is higher, then the case temperature will be higher.

iv) The temperature of the two types of power transistor is Germanium: 100°C to 110°C
Silicon : 150°C to 200°C Heat sinks increase the power rating (ie. power handling capacity) of a transistor by getting rid of the heat developed quickly.

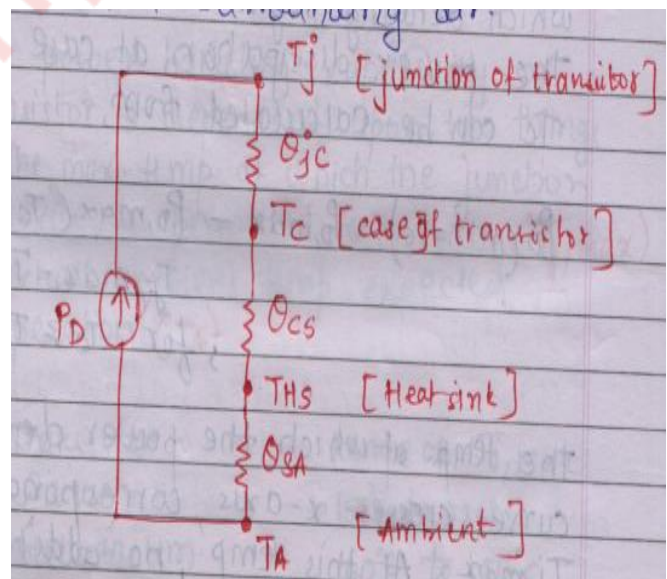
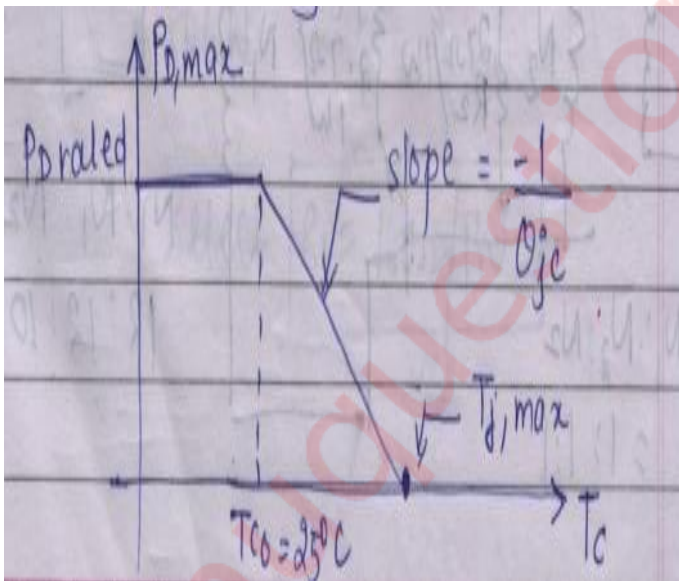
v) It is in the form of a sheet of metal. Since the power dissipation within a transistor is mainly due to power dissipated at collector junction, the collector (connected to the case of the transistor) is bolted on to metal sheet for faster radiation of heat.

vi) Sometimes the transistor is connected to a large heat sink with fins causing more efficient removal of heat from the transistor. When heat flows out of a transistor, it passes through the case transistor and into the heat sink, which then radiates the heat into the surrounding air.

viii) The temperature of the transistor case T_c will be slightly higher than the temperature of the heat sink which in turn is slightly higher than the ambient temperature T_A .

Ambient Temperature: The heat produced at the junction passed through the transistor case (metal or plastic housing) are radiates to the surrounding air. The temperature of this air is known as the ambient temperature.

ix) Power derating curve : A plot of maximum rated power of device versus case temperature of transistor is called as power derating curve of transistor.



d) Sketch symbol of n-channel and p-channel Depletion MOSFET . State giving reasons, why it is known as depletion MOSFET ? [5M]

Ans : i) The depletion type MOSFET transistor is equivalent to a “normally closed” switch. The depletion type of transistors requires gate – source voltage (V_{GS}) to switch OFF the device.



ii) The symbols for depletion mode of MOSFETs in both N-channel and P-channel types are shown above. In the above symbols we can observe that the fourth terminal substrate is connected to the ground, but in discrete MOSFETs it is connected to source terminal.

iii) The continuous thick line connected between the drain and source terminal represents the depletion type. The arrow symbol indicates the type of channel, such as N-channel or P-channel. In this type of MOSFETs a thin layer of silicon is deposited below the gate terminal. The depletion mode MOSFET transistors are generally ON at zero gate-source voltage (V_{GS}).

iv) The conductivity of the channel in depletion MOSFETs is less compared to the enhancement type of MOSFETs.

v) The various biasing circuits for D- MOSFET are :

- Zero Biasd Circuit
- Self Biasd
- Voltage Divider Biased