Linear Integrated Circuit
Sem 1V / ELTL / CHOICE BASED/DEC 2018 SOLUTION

Q.1 Attempt any 4 questions:

Q.1(a) With neat circuit explain the working of comparator circuit. [5]

Ans: A comparator as its name implies, compares a signal voltage on one input of an op-amp with

known voltage called a reference voltage on the other input.

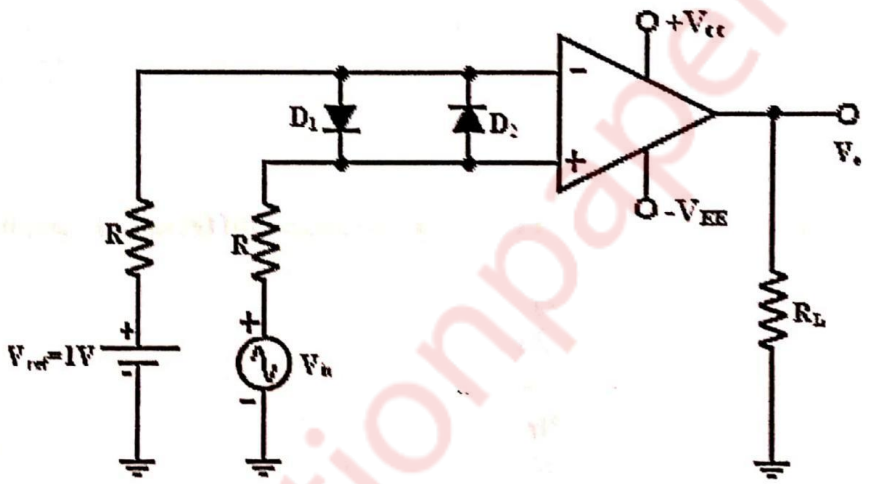
Comparators are used in circuits such as,

1)Digital Interfacing

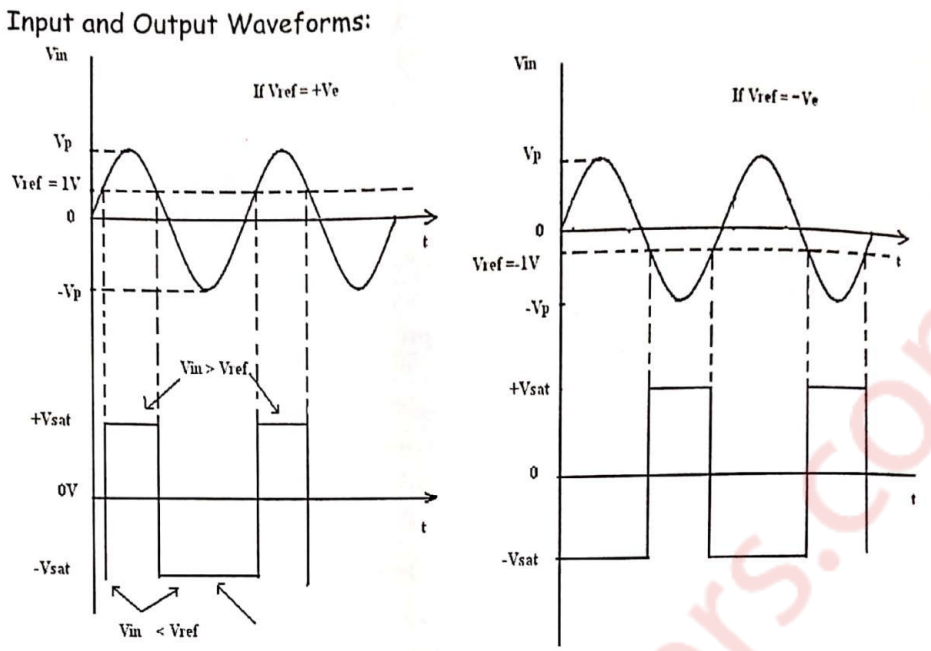
2) Schmitt Trigger

3)Discriminator

4) Voltage level detector and oscillators.



A fixed reference voltage Vrefof 1 V is applied to the negative terminal and time varying signal voltage Vin is applied to the positive terminal. When Vis less than Vref the output becomes Vo at - Vsat [Von Vref => V. (Vsat)]. When Vin is greater than Vref, the (+) input becomes positive, the Vo goes to +Vsat [Vin > Vref => Vo (+Vsat)]. Thus the Vo changes from one saturation level to another. The diodes D1 and D2 protects the op-amp from damage due to the excessive input voltage Vin. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes. The resistance R in series with Vin is used to limit the current through D1 and D2. To reduce offset problems, a resistance Rcomp = R is connected between the (-ve) input and Vref.



Q.1(b) Write short note on Bi-FET and Bi-MOS differential amplifier circuit. **[5]**

Ans:1) Bi MOSFET differential pair.

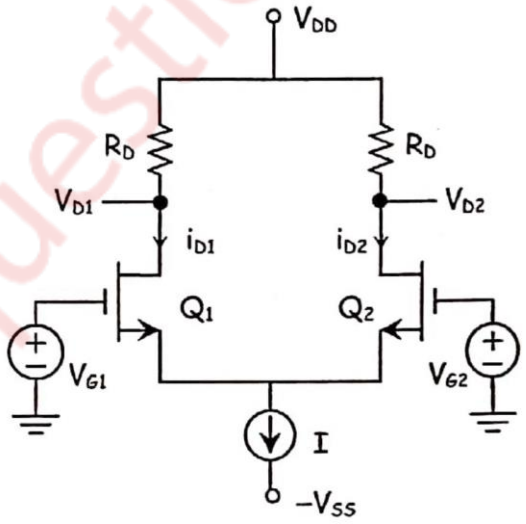


Fig) Bi MOSFET differential pair.

Fig. shows the basic MOSFET differential pair. Both the MOSFETs Q1 and Q2 are matched to each other in all respects.

I_Q is a constant current source similar to the one used for BJT differential amplifier. It has been used for biasing both the MOSFETs.

Both the MOSFETs are biased to operate in their saturation regions.

This current source also uses the dual polarity dc supply.

Hence even with $V_{GI} = V_{G2} = 0$, it is possible to bias both the MOSFETs in the saturation region. (Both of them will conduct even when $V_{GI} = V_{G2} = 0$,.)

2) Bi FET differential amplifier.

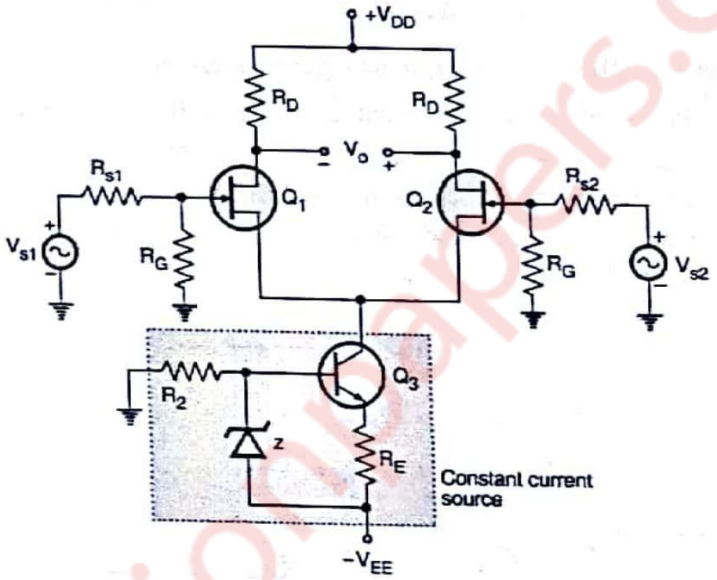


Fig) Bi FET differential amplifier.

In the differential amplifier configurations discussed so far we have used transistors, or MOSFETs.

But if we require very high input impedance, we can use JFETs in place of the transistors. For example, the dual input balanced output differential amplifier using JFETs is as shown in Fig.

The voltage-gain equations derived for these configurations using BJTs can also be used for the configurations using FET's except for the following replacements:

$R_C \rightarrow R_D$

$r_c \rightarrow 1/g_m$

The configuration shown in Fig. is a dual input balanced output differential amplifier. Hence the expression for the differential gain is given by.

$$A_d = \frac{Rc}{r_c}$$

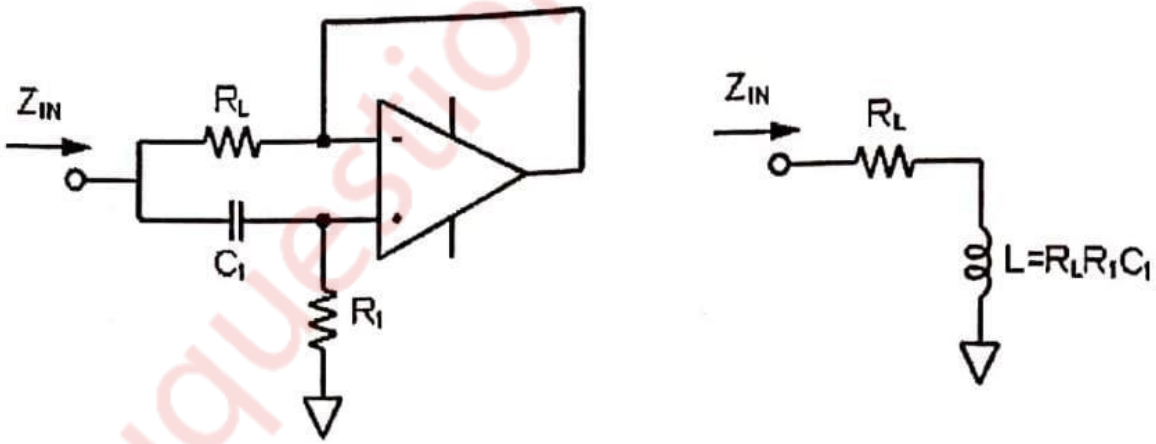
Replace Rc by R_D and by 1/gm to get,

$$Ad = g_m R_D$$

Q.1(c) Design a circuit with Op Amp. resistors and a capacitor that simulates an inductor of 1H. **[5]**

Ans: An inductor can be replaced by a much smaller assembly consisting of a capacitor, operational amplifiers or transistors, and resistors. This is especially useful in integrated circuit technology where building inductors from large loops of wire is impractical.

The circuit in Figure reverses the operation of a capacitor, thus making a simulated inductor. An inductor resists in its current, so when dc voltage is applied to an inductance, the current rises slowly. es slowly, and the voltage falls as the external resistance becomes more significant.



An inductor passes low frequencies more readily than high frequencies, the opposite of a capacitor. An ideal inductor has zero resistance. It passes dc without limitation, but it has infinite impedance at infinite frequency.

For the circuit in figure, if a DC voltage step is suddenly applied to the inverting input through resistor R_L, the op amp ignores the sudden step because the change is also coupled directly to the non-inverting input via C_1.The op amp

represents high impedance, just as an inductor does. As C_1 charges through R_L the voltage across R1 falls, so the op-amp draws current from the input through R_L. This continues as the capacitor charges, and eventually the op-amp has an input and output close to virtual ground because the lower end of R1 is connected to ground.

When C1 is fully charged, resistor R_L limits the current flow, and this appears as a series resistance within the simulated inductor. This series resistance limits the Q of the inductor. Real inductors generally have much less resistance than the simulated variety.

The value of the inductor is given by

$L = R_L R_1 C_1$

Let $R_L = R_1 = 1$ Kohms then,

$1 = 1K\ 1K.C_1$

$C_1 = 1$ uF

Q.1(d) For a regulated dc power supply the output voltage varies from 12 V to 11.6 V when the load current is varied from 0 to 100 mA which is the maximum value of I_L. If the ac line voltage and temperature are constant, calculate the load regulation, % load regulation and output resistance of the power supply. [5]

Ans: $\Delta Vo = 0.4V$, $\Delta I_L = 100$ mA

Load regulation: $\frac{\Delta Vo/Vo}{\Delta IL} = \frac{0.4/12}{100x10^{-3}}$

$V_L = \frac{R_L}{Ro+R_L} Vo$

$11.6 = \frac{R_L}{Ro+R_L} Vo$

$I_L = \frac{Vo}{Ro+R_L}$

$100x10^{-3} = \frac{12}{Ro+R_L}$

$Ro + R_L = 120$

From (1),

11.6 = $\frac{RL}{120}Vo$

11.6 = $\frac{RL}{120}12$

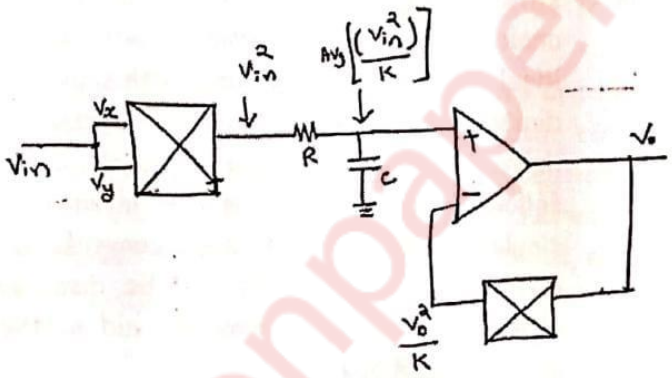
R_L=116 Ω

Ro +R_L = 120

Ro = 4 Ω

Q.1(e) How can the true RMS value of voltage signal to measured using analog multipliers. [5]

Ans:



By virtual short,

$\frac{Vo^2}{K}$ =Avg[(Vin)^2/K]

Vo = $\sqrt{Avg(Vin)^2}$

= RMS value of Vin

Q.2(a) Design an adjustable output voltage regulator circuits using IC 317 to give 5 to 12 volts at I_L 1 Amp. Given : I_{ADJ} =100 uA and let R_1 = 240 Ω

Ans.: [10]

I_{limit} = $\frac{1.25}{Rlimit}$

1A = $\frac{1.25}{Rlimit}$

R_{limit} = 1.25 Ω

Vol = (1 + $\frac{R2'}{R1}$)1.25+Idi R_2'

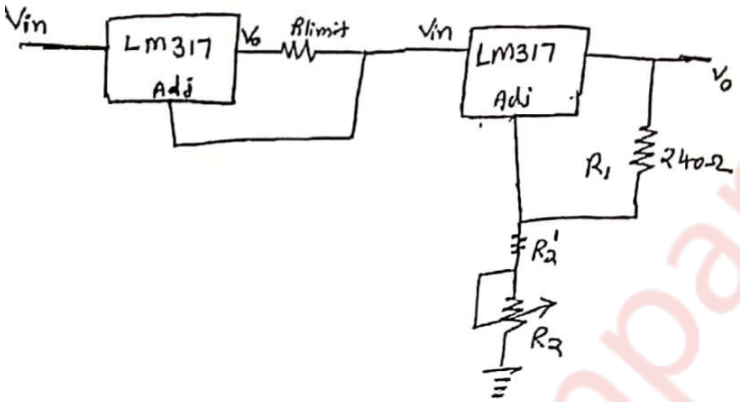
5 = = (1 + $\frac{R2'}{240}$)1.25+ 100 X $10^{-6}R_2$'

R_2' =937.5 Ω

Vo_H = (1 + $\frac{R2+R2'}{R1}$)1.25+Idj R_2'

12 = (1 + $\frac{R2+937.5'}{240}$)1.25+ 100 X 10^{-6}

R_2 = 1126.4808 Ω



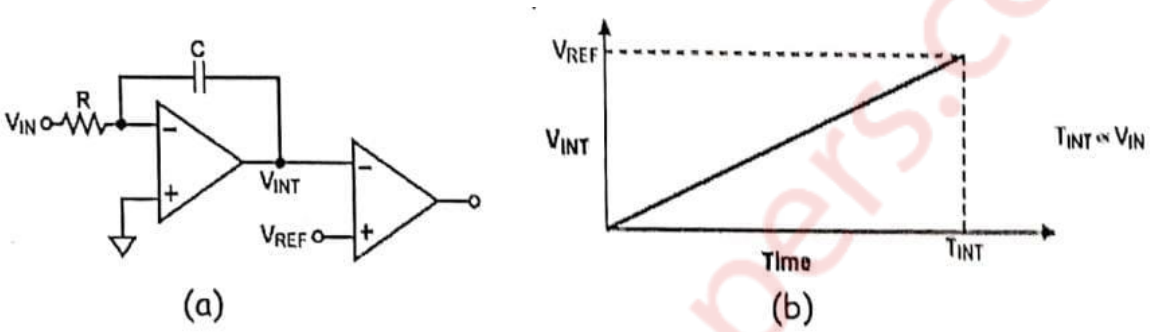
Q.2(b) Explain the operation of single slope integrating ADC and state its advantages, disadvantages. [10]

Ans.: Integrating analog-to-digital converters (ADCs) provide high resolution analog-to-digital conversions, with good noise rejection. These ADCs are ideal for digitizing low bandwidth signals, and are used in applications such as digital multimeters and panel meters. They often include LCD or LED drivers and can be used stand alone without a microcontroller host. The following article explains how integrating ADCs work. Discussions include single-, dual- and multi-slope conversions. Also, an in-depth analysis of the Integrating architecture will be discussed. Finally a comparisons against other ADC architectures will aid in the understanding and selection of integrating ADC.

Integrating analog-to-digital converters (ADCs) provide high resolution can provide good line frequency and noise rejection. Having started with ubiquitous 7106, these converters have been around for quite some time,The integrating architecture provides a novel yet straightforward approach to converting a low bandwidth analog signal into its digital representation. These type of converters

often include built-in drivers for LCD or LED displays and are found in many portable instrument applications, including digital panel meters and digital multimeters.

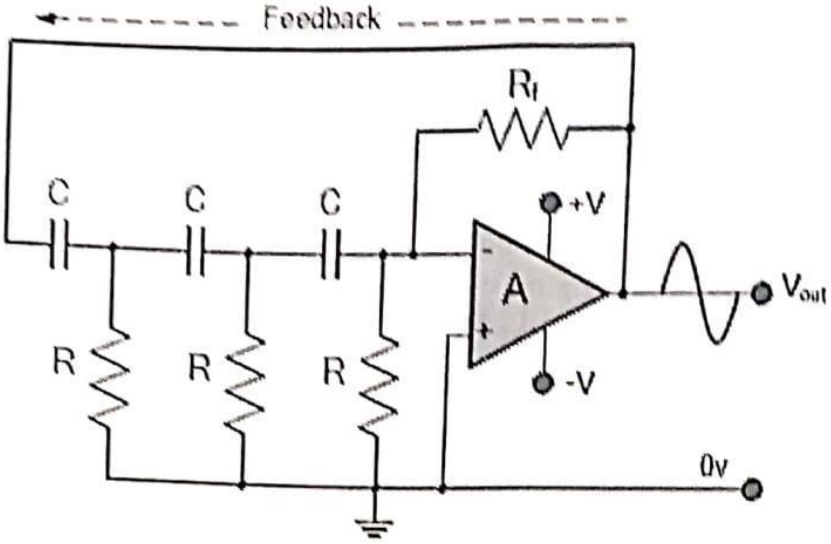
The simplest form of an integrating ADC uses a single-slope architecture as shown in figure. Here, an unknown input voltage is integrated and the value compared against a known reference value. The time it takes for the integrator to trip the comparator is proportional to the unknown voltage (TINT/VIN). In this case, the known reference voltage must be stable and accurate to guarantee the accuracy of the measurement.



One drawback to this approach is that the accuracy is also dependent on the tolerances of the integrator's R and values. Thus in a production environment, slight differences in each component value change the conversion result and make measurement repeatability quite difficult to attain. To overcome this sensitivity to the component values, the dual-slope integrating architecture is used.

Q.3(a) Draw a neat circuit diagram of a RC phase shift oscillator using op-amp. Derive its frequency of oscillation. What are the values of R and C for frequency of oscillation to be 1 kHz? [10]

Ans. When used as RC oscillators, Operational Amplifier RC Oscillators are more common than their bipolar transistors counterparts. The oscillator circuit consists of a negative-gain operational amplifier and a three section RC network that produces the 180" phase shift. The phase shift network is connected from the op-amps output back to its "inverting input as shown below.



As the feedback is connected to the inverting input, the operational amplifier is therefore connected in its "inverting amplifier" configuration which produces the required 180° phase shift while the RC network produces the other 180° phase shift at the required frequency (180° + 180").

Although it is possible to cascade together only two single-pole RC stages to provide the required 180° of phase shift (90°+90°), the stability of the oscillator at low frequencies is generally poor.

One of the most important features of an RC Oscillator is its frequency stability which is its ability to provide a constant frequency sine wave output under varying load conditions. By cascading three or even four RC stages together (4 x 45°), the stability of the oscillator can be greatly improved.

RC Oscillators with four stages are generally used because commonly available operational amplifiers come in quad IC packages so designing a 4 stage oscillator with 45° of phase shift relative to each other is relatively easy. RC Oscillators are stable and provide a well-shaped sine wave output with the frequency being proportional to 1/RC and therefore, a wider frequency range is possible when using a variable capacitor. However, RC Oscillators are restricted to frequency applications because of their bandwidth limitations to produce the desired phase shift at high frequencies.

Q.3(b) Explain the working principle of successive approximation type ADC. [10]

Ans. Successive Approximation type ADC is the most widely used and popular ADC method. The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digital

output, unlike the counter and continuous type A/D converters. The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB. The principle of successive approximation process for a 4-bit conversion is explained here. This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

(1) The MSB is initially set to 1 with the remaining three bits set as 000.

The digital equivalent voltage is compared with the unknown analog input voltage.

(2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to O and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example.

Let us assume that the 4-bit ADC is used and the analog input voltage is V_A

11 V. when the conversion starts, the MSB bit is set to 1.

Now VA = 11V > Vo = 8V = $[1000]^2$

Since the unknown analog input voltage VA is higher than the equivalent digital voltage VD, as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows:

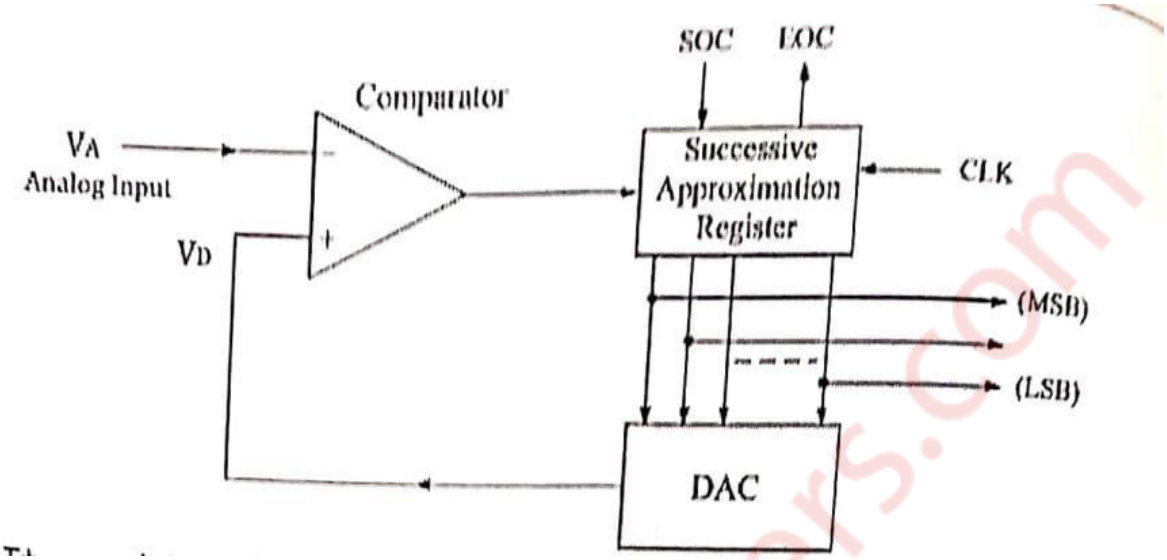
Vo = 12V = $[1100]^2$

Now VA = 11V< V_D = 12V = $[1000]^2$

Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage VD. As discussed in step (2), the second MSB is set to O and next MSB set to 1 as V_D = 10V = $[1100]^2$Now again VA = 11V > V_D = 10V = $[1100]^2$

Again as discussed in step (2) VA > Vo, hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is Vo = 11V = $[1011]^2$ Now finally VA = V_D, and the conversion stops.

The functional block diagram of successive approximation type of ADC is shown below



It consists of a successive approximation register (SAR). DAC comparator. The output of SAR is given to n-bit DAC, The equivalent and output voltage of DAC, Vo is applied to the non-inverting input of the comparator. The second input to the comparator is the unknown analog input voltage VA. The output of the comparator is used to activate the successive approximation logic of SAR.

When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.

Advantages:

1. Conversion time is very small

2. Conversion time is constant and independent of the amplitude of the analog input signal V

Disadvantages:

1. Circuit is complex.

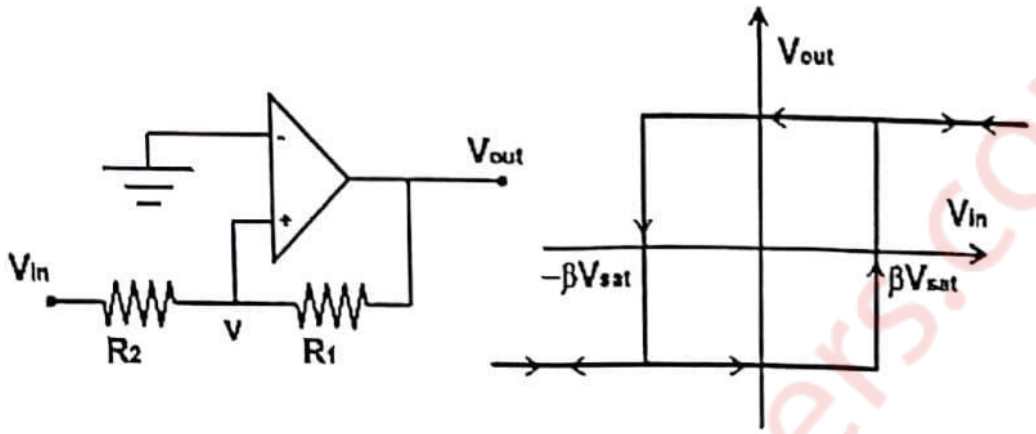
2. The conversion time is more compared to flash type ADC,

Q.4(a) With the help of a neat diagram, input and output waveforms and voltage transfer characteristics explain the working of non-inverting Schmitt trigger. Derive the expressions for its threshold levels. Explain how these levels can be varied? [10]

Ans:- In a Schmitt trigger , the Voltages at which the output at which the output switches from +Vsat to -Vsat or vice versa are called upper trigger point (UTP)

and lower trigger point (LTP). The difference between the two trip points is called hysteresis.

In case of Non-inverting Schmitt trigger the feedback is given at non inverting terminal, The inverting terminal is grounded and the input voltage is connected to non-inverting input. The figure shows a non-inverting Schmitt trigger circuit,



To analyze the circuit behaviour, let us assume the output is negatively saturated. Then the feedback voltage is also negative (-Vsat). Then the feedback voltage is also negative. This feedback voltage will hold the output in negative saturation until the input voltage becomes positive enough to make voltage positive.

$$V_+ = \frac{(-V_{sat} - V_{in})}{R_1 + R_2} R_2 + V_{in} = \frac{R_1}{R_1 + R_2}\left[\frac{-R_2 V_{sat}}{R_1} + V_{in}\right]$$

When Vin becomes positive and its magnitude is greater than (Rz/R_1) Vset, then the output switches to +Vsat. Therefore, the UTP at which the output switches to +Vsat is given by

UTP = R_2V/R_1

$$V_+ = \frac{(V_{sat} - V_{in})}{R_1 + R_2} R_2 + V_{in} = \frac{R_1}{R_1 + R_2}\left[\frac{R_2 V_{sat}}{R_1} + V_{in}\right]$$

When Vin becomes negative and its magnitude is greater than (Rz/R) Vsat.

then the output switches to -Vsat. Therefore,

LTP = $-\frac{R2Vsat}{R1}$

The difference of UTP and LTP gives the hysteresis of the Schmitt trigger.

Vhs= UTP – LTP = $2\frac{R2}{R1}V_{sat}$

Q.4(b) Design a differentiator to differentiate an input signal that vary in frequency from 10 Hz to about 500 Hz. Draw its frequency response. If a sine wave of 2 V peak at 500 Hz is applied to the differentiator, write expression for its output and draw output waveform.

Ans:

Frequency range : 10 Hz to 500 Hz

Peak values = 2V, f = 500 Hz

fa = 500 Hz (Highest frequency)

C1 = 0.1 uF

fa = $\frac{1}{2\pi R_f C_1}$

Rf = $\frac{1}{2\pi\ X\ 0.1\ X\ 10^{-6} X\ 500}$ = 3.183 kΩ

fb = $\frac{1}{2\pi R_1 C_1}$

R_1 = $\frac{1}{2\pi f b C_1}$ = 159.15 Ω

R1C1 = Rf Cf

Cf = 5nF

Rcomp = 3.2KΩ

Vi = 2sin(2π 500t)

= 2sin(1000πt)

Vo = -RfC1$\frac{dVi}{dt}$

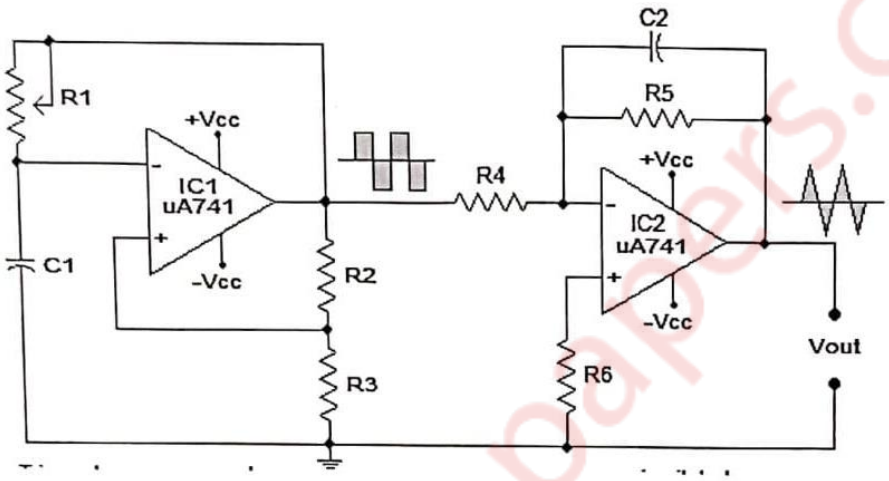
= -3.2 X 10^3 X 0.1X 10^{-6} $\frac{d[2\sin 1000\pi t\}}{dt}$

= -2cos(1000πt)

Q.5(a) Draw the circuit diagram of a square and triangular waveform generator using op-amp. With the help of waveforms at suitable points in the circuit explain its working. Explain how duty cycle can be varied? [10]

Ans.

The circuit using an Op Amp based square wave generator for producing the square wave and an Op amp based integrator for integrating the square wave is shown below:



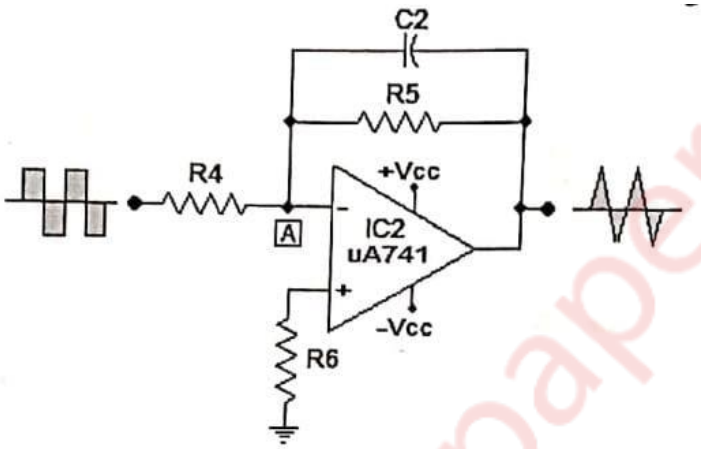
The square wave generator is based on a uA741 Op Amp (IC_1). Resistor R, and capacitor C1 determines the frequency of the square wave, Resistor R2 and R3, forms a voltage divider setup which feedbacks a fixed fraction of the output to the non-inverting input of the IC.

Initially, when power is not applied the voltage across the capacitor C1 is 0.

When the power supply is switched ON, the resistor R1 and the output of the Opamp will be high +(Vcc.). A fraction of this high voltage is fed back to the non- inverting pin by the resistor network R2. R3. When the voltage across the charging capacitor is increased to a point the voltage at the inverting pin is higher than the non-inverting pin, the output of the Opamp swings to negative saturation (-Vcc). The capacitor quickly discharges through R, and starts charging in the negative direction again through R1. Now a fraction of the negative high output (-Vcc) is fed back to the non-inverting pin by the feedback network R2, R3. When the voltage across the capacitor has become so negative that the voltage at the inverting pin is less than the voltage at the non-inverting pin, the output of the Opamp swings back to the positive saturation. Now the capacitor discharges through Ri and starts charging in positive direction. This

cycle is repeated over time and the result is a square wave swinging between Vcc and starts charging through the -Vcc at the output of the Opamp.

Next part of the triangular wave generator is the opamp integrator. Instead of using a simple passive RC integrator, an active integrator based on opamp is used here. The op amp IC used in this stage is also HA 741 (IC). Resistor R, in conjunction with Ra sets the gain of the integrator and resistor Rs in conjunction with Cz sets the bandwidth. The square wave signal is applied to the inverting input of the opamp through the input resistor R4. The opamp integrator part of the circuit is shown in the figure below:

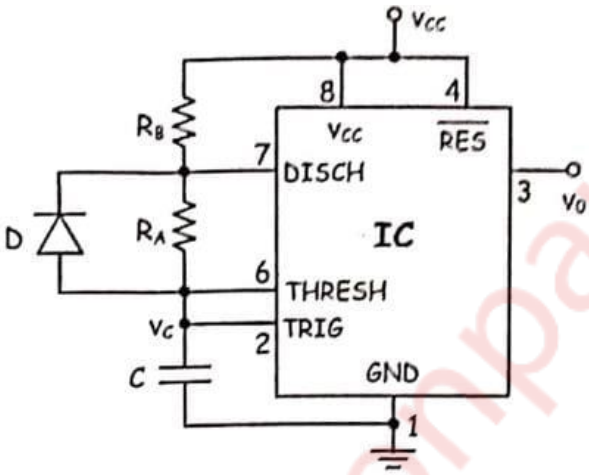


Let's assume the positive side of the square wave is first applied to the integrator. By virtue capacitor C2 offers very low resistance to this sudden shoot in the input and C2 behaves something like a short circuit. The feedback resistor R: connected in parallel to C can be put aside because Rs has almost zero resistance at the moment. A serious amount of current flows through the input resistor R4 and the capacitor C2 bypasses all these current. As a result the inverting input terminal (tagged A) of the opamp behaves like a virtual ground because all the current flowing into it is drained by the capacitor C2. The gain of the entire circuit (Xc_2/R_4) will be very low and the entire voltage gain of the circuit will be close to the zero.

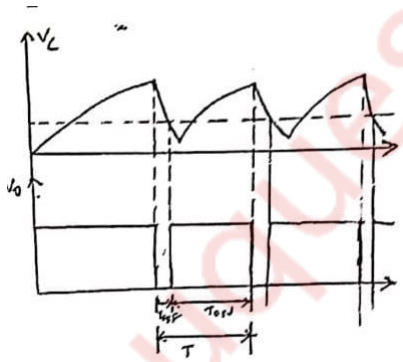
After this initial "kick" the capacitor starts charging and it creates an opposition to the input current flowing through the input resistor R4. The negative feedback compels the op amp to produce a voltage at its out so that it maintains the virtual ground at the inverting input. Since the capacitor is charging its impedance Xc keeps increasing and the gain Xc_2/R_4 also keeps increasing. This results in a ramp at the output of the op amp that increases in a rate proportional to the RC time constant ($T= R_4C_2$) and this ramp increases in amplitude until the capacitor is fully charged.

When the input to the integrator (square wave) falls to the negative peak the capacitor quickly discharges through the input resistor R4, and starts charging in the opposite polarity. Now the conditions are reversed and the output of the opamp will be a ramp that is going to the negative side at a rate proportional to the R_4R_2 time constant. This cycle is repeated and the result will be a triangular waveform at the output of the opamp integrator.

Q.5(b) Analyze the circuit given in Figure. Draw the waveforms at output terminal vo and across the capacitor C. Comment on the duty cycle of output waveform. Take diode D as an ideal diode and assume R_A is equal to R_B. [10]



Ans:



T_{OFF} = 0.693 RoC

Ro – Resistance of forward biased diode.

T_{ON} = 0.693(Ra +Rb)C

D = $\frac{Ton}{Ton+Toff} X\ 100$

$$= \frac{0.693(Ra + Rb)C}{0.693(Ra + Rb)C + 0.693\ RoC} X\ 100$$

R_O = 0 for idel diode

D = 100%

Q6) Write a short note on (any four) : [20]

Q 6(a) Write a short note on Wilson Current source. [5]

Ans:

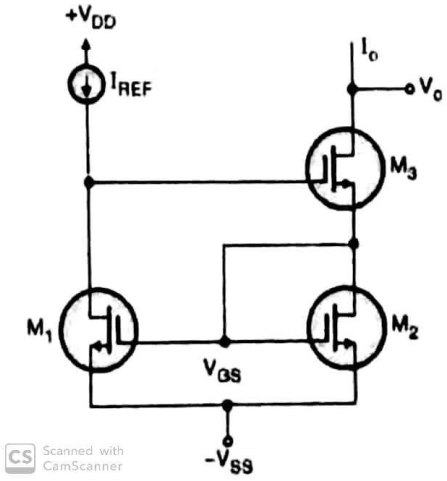


Fig 1) The Wilson MOS mirror

Fig 1 shows the MOS version of Wilson current mirror. The MOS Wilson mirror has a higher value of Ro as compared to that of the bipolar Wilson mirror . The V_{ds} values of M1 and M2 in this circuit are not equal to wach other. Also $\lambda \neq 0$. Hence the ratio of Io and I_{Ref} is slightly different from the aspect ratios. The basic structure and principle of operation of the Wilson MOS mirror is same as that of the BJT Wilson mirror

Output resistance (Ro):

Fig2 shows the small signal equivalent circuit. The output resistance Ro of the Wilson current is approximately equal to zero. Ro $= g_{m3} r_{o3}\ r_{o2}$

As can be seen this value is same as the output resistance of the cascode current mirror circuit.

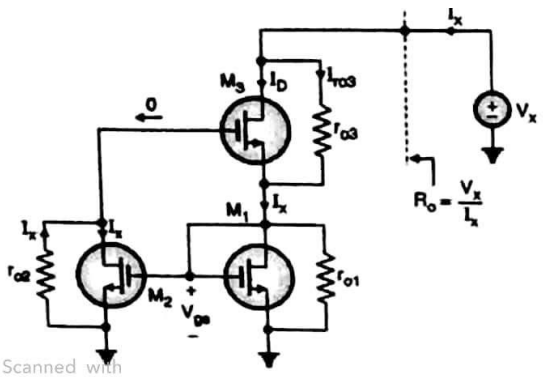
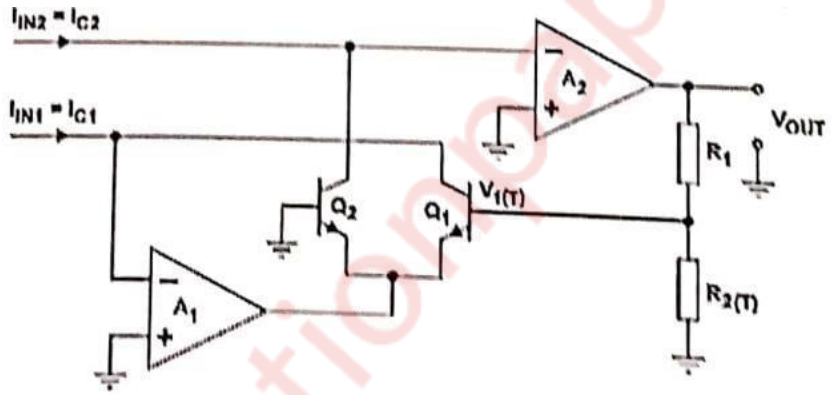


Fig. 1.11(b) : Analysis to determine the output resistance

Q 6(b). Write a short note on temperature compensated log amplifier. [5]

Ans:



To avoid output changes due to temperature, the temperature-compensated log amp in Figure is required. Here, generating the difference of two logarithms eliminates Ies. From the previous example, we take the logarithmic relationship between the basis-emitter voltage. V_{Be}, and the collector current, Ic, for both transistors, Q1 and Q2:

$V_{BE1} = V_T \times \text{In} \frac{Ic1}{Ies1}$ and $V_{Be2} = Vt \times \text{In} \frac{Ic2}{Ies2}$

The two logging transistors build a difference amplifier whose output voltage, V1. yields the difference of both base-emitter voltages:

$V_1 = V_{B1} - V_{BE2}$

$= V_T \text{ x In } \frac{Ic1}{Ies1} - Vt \text{ x In } \frac{Ic2}{Ies2}$

With matched and isothermal transistors, Ies1 = Ies2 = Is, and Equation simplifies to

$V_{I(T)} = V_T \text{ x In } \frac{Ic1}{Ic2}$

A remaining temperature dependency exists via only V_T. Via the voltage divider, R1 and R2, V1 Represents only a part of the entire circuit output voltage, Vout

$Vout(T) = (1+ \frac{R1}{R2}) \text{ x } V_1$

$= (1+ \frac{R1}{R2}) \text{ x } V_T \text{ x In } \frac{Ic1}{Ic2}$

To compensate for the effect of V_T, R_Z is replaced by a temperature dependent resistor with a positive temperature coefficient. This keeps constant over a certain temperature range. Practical values for the temperature coefficient vary between 3500 and 3700 ppm/K During the manufacturing process of log amps, the internal components and the temperature coefficient are trimmed to a fixed value. In addition, the natural logarithm is converted to log10 by applying a correction factor.

n = 2.3, according to In x = 2.3 x log x. The expression $(1+ \frac{R1}{R2}) \text{ x } V_T \text{ x } 2.3$

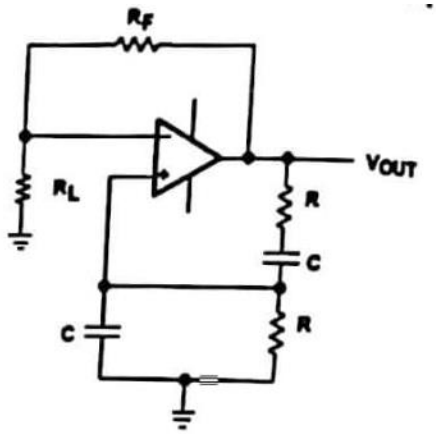
becomes a constant, q, with the unit V/decade, simplifying the computation

of Vout to $(1+ \frac{R1}{R2}) \text{ x } V_T$.

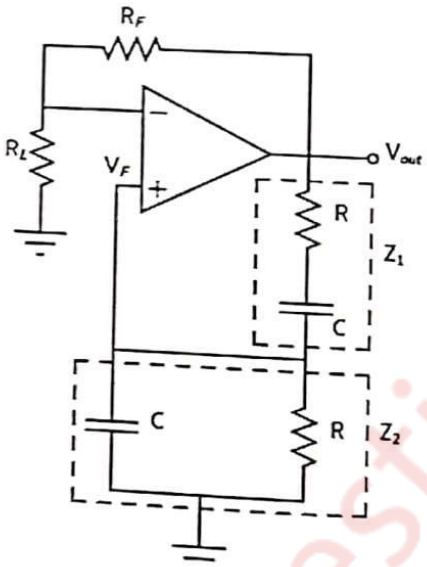
Q.6(c) Write a short note on Wein Bridge Oscillator. [5]

Ans: The Wien bridge oscillator is one of the simplest oscillator. Figure shows the basic Wien bridge circuit configuration OPAMP is used as the amplifying device and the Wien bridge is used as the feedback element. The OPAMP is used in non inverting mode that provides a phase shift of 0^0. One can expect that the phase shift introduced by the feedback network also to be equal to 0 at the frequency of oscillations. The frequency of oscillations is,

f = $\frac{1}{2\pi RC}$



The feedback network provides gain of 1/3. Hence, the amplifier gain in inverting mode should be slightly greater than 3.



The condition for sustained oscillation and the oscillating frequency is given by the feedback voltage Vf is given by.

Vf = $\frac{Z1}{Z1+z2}\ Vout$

Where Z1 = $\frac{R}{1+RCS}$ and Z2 = R + $\frac{1}{CS}$

Substituting the values in the above equation we get,

Vf = $\frac{\frac{R}{1+RCS}}{\frac{R}{1+RCS}+\ R+\frac{1}{CS}}$Vout

Substituting the values of s=jω and simplifying we get ,

$$Vf = \frac{j\omega CR}{1+3RCj\omega - C^2R^2\omega^2} Vout$$

To ensure phase shift of 0^o by the feedback network,

$$1 - C^2R^2\omega^2 = 0$$

Thus $\omega = 1/RC$, $F=1/2\pi RC$

Which happens for $Vf = \frac{Vout}{3}$

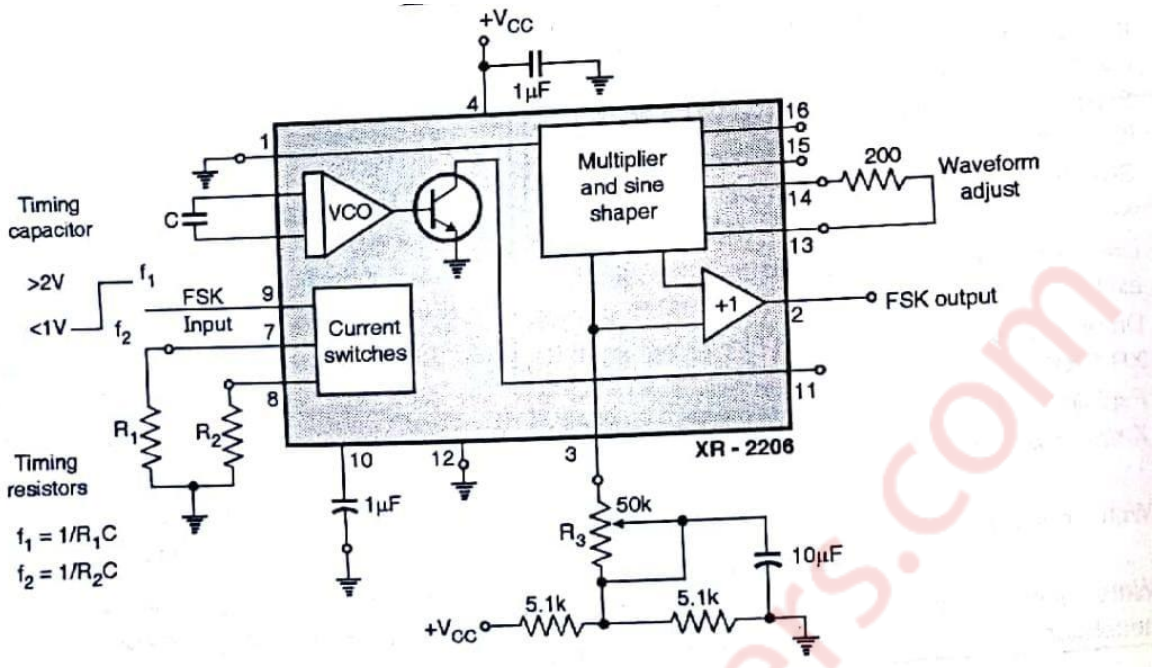
This implies that the non inverting gain of the amplifier should be slightly greater than 3 so that the loop gain condition is satisfied

Q.6(d) Write short note on XR2206 waveform generator. [5]

Ans: The XR-2206 is a monolithic function generator Integrated circuit capable of producing high quality square, triangle, sine, pulse and ramp waveforms of accuracy and high-stability. The output waveforms can be both frequency and amplitude modulated by an external voltage. Frequency of operation can be externally selected over a range of 0.01 Hz to more than 1 MHz. The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, frequency modulation, amplitude modulation or frequency shift keying generation XR-2206 has a typical drift specification of 20 ppm/°C The oscillator frequency can be linearly swept over a range of 2000:1 frequency with an external control voltage, while maintaining low distortion

Features of XR-2206

- Low-Sine Wave Distortion (THD 0.5%), insensitive to signal sweep
- Linear Amplitude Modulation Wide Supply Range (10 V to 26 V)
- Excellent Temperature Stability (20 ppm/ °C typical)
- Low-Supply Sensitivity (0.01%V, typical)
- TTL Compatible Frequency shift keying Controls
- Adjustable Duty Cycle (1% to 99%)



A sine-shaping network makes the triangular signal of the VCO, a sinusoidal signal that can be picked up at the pin 2. At pin 3 to set the exact medium voltage and the output amplitude. The additional output at pin 11 also delivers a square wave with the same frequency

The actual sample structure differs in some details from the data sheet.Thus, only a frequency ratio of 1 was chosen to 100, so a finer adjustment is possible. With the frequency determining capacitor of 0.1 uF an adjustment range of 100 Hz is reached to 10 kHz The frequency is changed by using a variable resistor.

The amplitude setting at pin 3 is connected with fixed resistors, output voltage is always the same. The switching sine / triangle was achieved with a jumper. On the board, the outputs of the circuit were placed in small wire loops, where the signals can be picked up directly with alligator clips.

Q.6(e) Write short note on switch mode power supply. [5]

Ans: A switched made power supply (SMPS) is an electric circuit that converts power using switching devices that are turned on and off at high frequencies, and storage components such as Inductors or capacitors supply power when the switching device is in its non-conducting state.

Switching power supplies have high efficiency and are widely used in a variety of electronic equipment, including computers and other sensitive equipment requiring stable and efficient power supply. A switched-mode power supply is also known es a switch-made power supply or switching-mode power supply.

Switched-mode power supplies are classified according to the type of input and output voltages. The four major categories are:

- AC to DC
- DC to AC
- DC to DC
- AC to AC

A basic isolated AC to DC switched-mode power supply consists of

- Input rectifier and filter
- Inverter consisting of switching devices such as MOSFET's
- Transformer
- Output rectifier and filter
- Feedback and control circuit

The input DC supply from a rectifier or battery is fed to the inverter where it is turned on and off at high frequencies of between 20 KHz and 200 KHz by the switching MOSFET or power transistors. The high-frequency voltage pulses from the inverter are fed to the transformer primary winding, and the secondary AC output is rectified and smoothed to produce the required DC voltages. A feedback circuit monitors the output voltage and instructs the control circuit to adjust the duty cycle to maintain the output at the desired level.

There are different circuit configurations known as topologies, each having unique characteristics, advantages and modes of operation, which determines how the input power is transferred to the output. Most of the commonly used topologies such as flyback, push-pull, half bridge bridge and full bridge, consist of a transformer to provide isolation, voltage scaling, and multiple output voltages. The non-isolated configurations do not have a Transformer and the power conversion is provided by the inductive energy transfer.

Advantages of switched-mode power supplies

- Higher efficiency of 68% to 90%
- Regulated and reliable outputs regardless of variations in input supply voltage
- Small size and lighter Flexible technology High power density

Disadvantages:

- Generate electromagnetic interference
- Complex circuit design
- Expensive compared to linear supplies
- Switched-mode power supplies are used to power a wide variety of equipment such as computers, sensitive electronics, battery-operated devices and other equipment requiring high efficiency

□ □ □ □