Q.P. CODE : 57446

MUMBAI UNIVERSITY

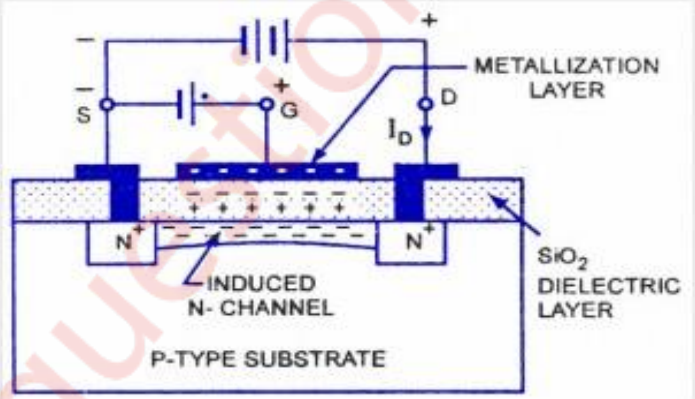
ELECTRONICS DEVICES & CIRCUITS–II

Semester 4 – December 18 – Choice Base

Q.1 a) Draw a neat labelled diagram of Enhancement Type MOSFET and explain its operation. **[20M]**

Ans : i) MOSFET are metal oxide surface field effect transistor.There are two types of MOSFETS: depletion-type MOSFETs and enhancement-type MOSFETs.

ii) Enhancement type MOSFET operates only in the *enhancement mode* and has no depletion mode. It operates with large positive gate voltage only. It does not conduct when the gate-source voltage $V_{GS} = 0$. This is the reason that it is called normally-off MOSFET. In these MOSFET's drain current I_D flows only when V_{GS} exceeds V_{GST} [gate-to-source threshold voltage].



Operation of N-Channel E-MOSFET

iii)When drain is applied with positive voltage with respect to source and no potential is applied to the gate two N-regions and one P-substrate from two P-N junctions connected back to back with a resistance of the P-substrate. So a very small drain current that is, reverse leakage current flows. If the P-type substrate is now connected to the source

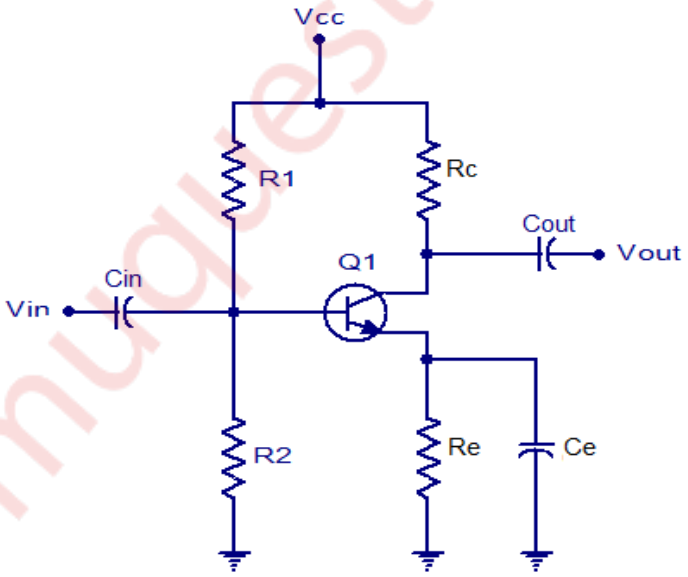
terminal, there is zero voltage across the source substrate junction, and the drain-substrate junction remains reverse biased.

iv) When the gate is made positive with respect to the source and the substrate, negative (i.e. minority) charge carriers within the substrate are attracted to the positive gate and accumulate close to the-surface of the substrate. As the gate voltage is increased, more and more electrons accumulate under the gate. Since these electrons can not flow across the insulated layer of silicon dioxide to the gate, so they accumulate at the surface of the substrate just below the gate.

v) These accumulated minority charge carriers N -type channel stretching from drain to source. When this occurs, a channel is induced by forming what is termed an inversion layer (N-type). Now a drain current start flowing. The strength of the drain current depends upon the channel resistance which, in turn, depends upon the number of charge carriers attracted to the positive gate. Thus drain current is controlled by the gate potential.

b) Explain RC coupled Amplifier.

Ans : i) A single stage common emitter RC coupled amplifier is a simple and elementary amplifier circuit. The main purpose of this circuit is pre-amplification that is to make weak signals to be stronger enough for further amplification. If designed properly, this RC coupled amplifier can provide excellent signal characteristics.



RC COUPLED AMPLIFIER

ii)The capacitor Cin at the input acts as a filter which is used to block the DC voltage and allow only AC voltage to the transistor. If any external DC voltage reaches the base of the transistor, it will alter the biasing conditions and affects the performance of the amplifier.

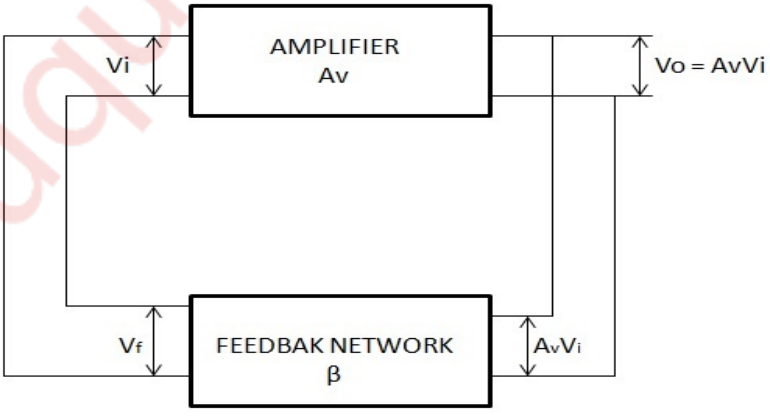
iii) R1 and R2 resistors are used for providing proper biasing to the bipolar transistor. R1 and R2 form a biasing network which provides necessary base voltage to drive the transistor in active region.

iv) The region between cut off and saturation region is known as active region. The region where the bipolar transistor operation is completely switched off is known as cut off region and the region where the transistor is completely switched on is known as saturation region.

v) Resistors Rc and Re are used to drop voltage of Vcc. Resistor Rc are a collector resistor and Re is emitter resistor. Both are selected in such a way that both should drop Vcc voltage by 50% in the above circuit. The emitter capacitor Ce and emitter resistor Re makes a negative feedback for making the circuit operation more stable.

c) What is oscillator ? Explain basic principles of an Oscillator.

Ans: i) An oscillator is an electronic circuit that generates sinusoidal oscillations known as sinusoidal oscillator. It converts input energy from a DC source into AC output energy of periodic waveform, at a specific frequency and is known amplitude. The characteristic feature of the oscillator is that it maintains its AC output.



ii) A sinusoidal oscillator is essentially a form of feedback amplifier, where special requirements are placed on the voltage gain $\mathbf{A_v}$ and the feedback networks $\boldsymbol{\beta}$.

iii) The oscillator ckt works on barkhauson's criteria, which states that an amplifier can be converted into an oscillator provided that following conditions must be satisfied.

--- Amplifier must have positive f/b

--- The Total Phase shift of the loop or circuit must be 3600 phase shift. The amplifier provides 1800 phase shift and the feedback network provides another 1800 phase shift. so the total phase shift of the circuit is 3600 phase shift.

--- | AB | ≥ 1 i.e. Loop gain value should be greater than or equal to one.

d) Differentiate Class A ,Class B and Class C Power Amplifiers.

Ans :

	Class A Power Amp.	Class B Power Amp.	Class C Power Amp.
1.	In this amplifier , the operating point of BJT is at centre of loadline.	In this amplifier, operating point of BJT is in cut off region.	In this amplifier,operating point point of BJT is below cut of region.
2.	Conduction angle lies in between 0 to 360 deg.	Conduction angle lies in between 0 to 180 deg.	Conduction angle lies in less than 90 deg.
3.	Overall efficiency of Class A power amplifier is poor. (25 % to 30 %)	Overall efficiency of Class B power amplifier is better. (70 % to 80 %)	Overall efficiency of Class C power amplifier is higher. (more than 80 %)
4.	Collector current flows at all times during full cycle of signal.	Collector current flows only during positive half cycle of input signal.	Collector current flows for less than half cycle of input signal.
5.	To achieve high linearity and gain, the output stage of a class A amplifier is biased “ON” (conducting) all the time	Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier	The Class C Amplifier design has the greatest efficiency but the poorest linearity of the classes of amplifiers
6.	As a class A amplifier operates in the linear portion of its characteristic curves, the single output	In the class B amplifier, there is no DC base bias current as its quiescent current is zero, so that the	the output signals amplitude and phase are linearly related to the input signals amplitude and phase

	device conducts through a full 360 degrees of the output waveform	dc power is small and therefore its efficiency is much higher than that of the class A amplifier	

Q.2 a) Design a two stage RC coupled CS-CE Amplifier to meet following specifications:

Av≥ 500 , $S \leq 8, Ri \geq 1M\Omega$, $Vcc = 6V$.

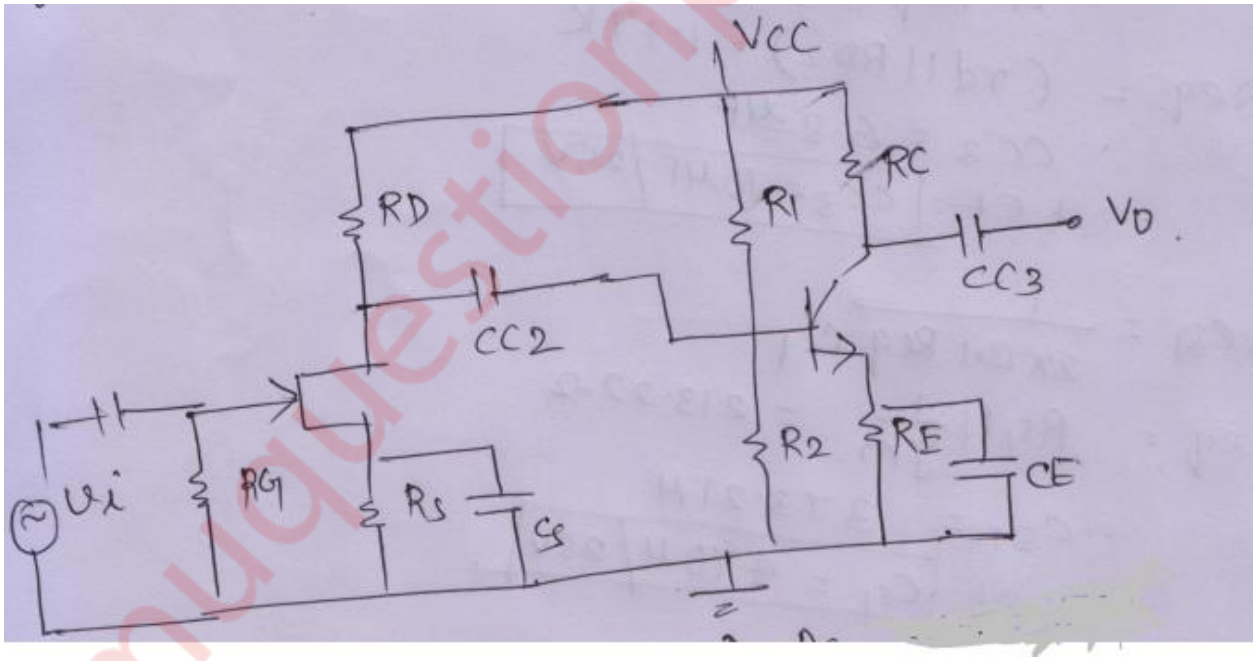
Assume the following data : $\beta(typ) = 290, hie = 4.5K\Omega, gmo = 5000\mu\mho, I_{DSS} = 7mA$,

$r_d = 50K$,Vp=-4V. **[15M]**

Ans : i) Given Specification : CS-CE Amplifier with gain of less than 500.Since input impedance is in $M\Omega$ first stage is common source JFET Amplifier and second stage is common emmiter BJT amplifier.This both stages are RC coupled .

ii) Let the transistor used be BC 147B and BFW11.

iii) Circuit Diagram :



iv) Specifications of transistors :

A) BFW 11 : - $gmo = 5000\mu\mho, I_{DSS} = 7mA, r_d = 50K$,Vp=-4V.

B) BC 147B : - hie = 4.5K , V(CE sat) = 0.25 V , $\beta(typ) = 290$

v) Let Av' = 5 and Av'' = 100 where Av' = Gain of first stage and Av''= Gain of second stage. Here we know that ,

$$Av'' = \frac{hfe(min).Rc}{hie} = \frac{240 \times Rc}{4.5K} = 1.87\ K\Omega$$

Choosing HSV , Rc = 2K Ω/0.25 W

vi) Q-point : V(CEQ)=Vcc/2 = 6/2 = 3 V

Let V(RE) = 10 % .Vcc = 0.6 V

Applying KVL in input loop ,

Vcc – Ic.Rc – V(CE) – V(RE) = 0

I(CQ) = 1.2 mA

RE = V(RE)/Ic = 0.6 / 1.2 = 0.5 KΩ / 0.25 W

vii) Now lets find R1 & R2 using stability factor , S= 8

We know that , $S = 1 + \frac{Rth}{RE} = 8$ => Rth = 3.5 KΩ

Applying KVL in second stage input assuming thevenins equivalent circuit,

$$Vth - \frac{Ic}{hFE} . Rth - V(BE) - V(RE) = 0$$

Vth = 1.314 V

But we know that using thevenins rule ,

$$Vth = \frac{R2}{R1+R2} . Vcc \quad \& \quad Rth = R1||R2$$

On solving this , we will get , R1 = 16KΩ / 0.25 W & R2 = 4KΩ / 0.25 W

viii) Now let us assume first stage , Av' = gm.(rd||RD||Rth||hie)

Considering midpoint biasing , I(DS) = I(DSS)/2 = 3.5 mA

But , $I(DS) = I(DSS).\left[1 - \frac{V(GS)}{Vp}\right]^2$

$3.5m = 7m.\left[1 - \frac{V(GS)}{-4}\right]^2$

V(GS) = -1.17 V

Now $gm = gmo\left[1 - \frac{V(GS)}{Vp}\right]$ => gm = 3.53 m℧

Hence gain expression :

Av' = gm.(rd||RD||Rth||hie)

= (3.53m).(50K||RD||3.5K||4.5K)

RD = 4 $K\Omega$ / 0.25W

ix) Applying KVL in loop , -V(GS) – ID.Rs = 0

Rs = 330 Ω/0.25 W

x) To find capacitance used in circuits : Let us assume fL =20 Hz

fL(cc1) = $\frac{1}{2\pi Req.cc1}$ => Req = Rg = 1M Ω => cc1 = 10 nF / 25V

fL(cc2) = $\frac{1}{2\pi Req.cc2}$ => Req = (rd ||Rd) + (Rth||hie)

cc2 = 2.2 uF / 25 V

fL(cc3) = $\frac{1}{2\pi Req.cc3}$ => Req = Rc = 2K Ω

cc3 = 4.4 uF / 25 V

fL(cs) = $\frac{1}{2\pi\ 0.1\ Req.cs}$ => Req = Rs ||(1/gm)

cs = 690 uF / 25 V

fL(ce) = $\frac{1}{2\pi\ 0.1 Req.ce}$ => Req = $\frac{RD||rd||Rth+hie}{1+hFE}$

ce = 4.7Mf / 25 V

b) For a 'n' stage cascaded amplifier,show that overall lower 3 dB cut-off frequency is

$$f_{LT} = \frac{f_L}{\sqrt{2^{1/n}-1}}.$$ **[5M]**

Ans : We know that for 'n' stage cascaded amplifier ,

$$\left(\frac{1}{\sqrt{1+\left(\frac{fL}{fL(n)}\right)^2}}\right)^n = \frac{1}{\sqrt{2}}$$

$$\therefore \left(\sqrt{1+\left(\frac{fL}{fL(n)}\right)^2}\right)^n = \sqrt{2}$$

Squaring on both sides and taking nth root,

$$\therefore \quad 2^{1/n} = 1+\left(\frac{fL}{fL(n)}\right)^2$$

$$\therefore \quad 2^{1/n} - 1 = \left(\frac{fL}{fL(n)}\right)^2$$

Taking square root on both side,

$$\therefore \quad \sqrt{2^{1/n} - 1} = \left(\frac{fL}{fL(n)}\right)$$

$$\therefore \quad f_{LT} = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

Where , fL(n) = Lower 3dB frequency of identical cascaded stages.

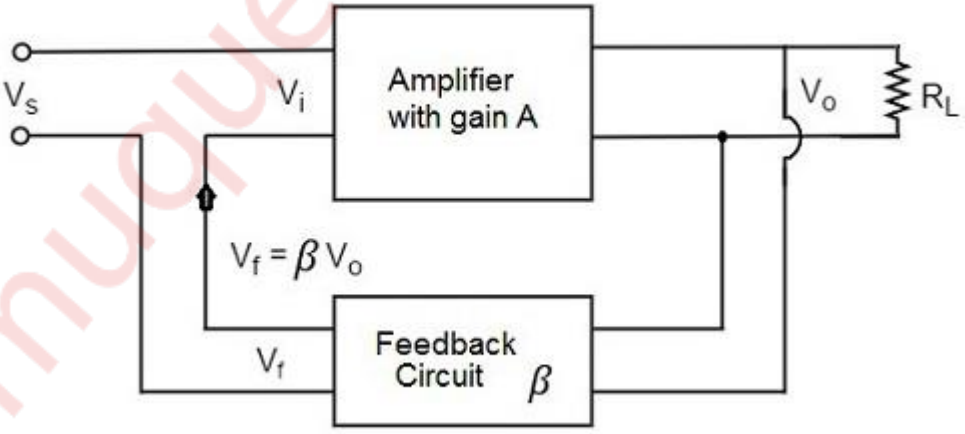
fL = Lower 3dB frequency of single stage

n =number of stages.

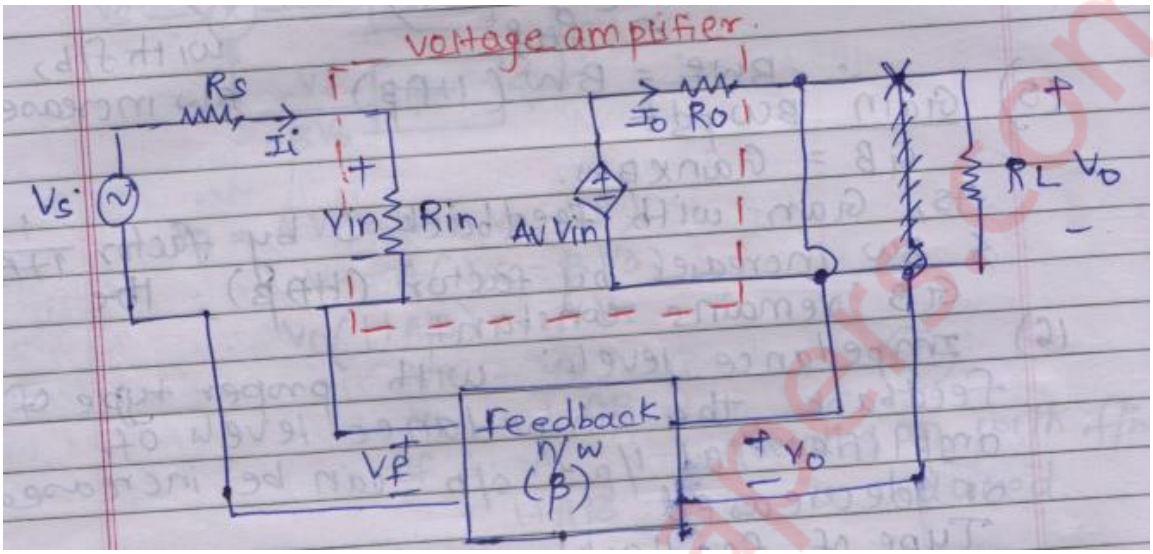
Q.3 a)With the help of neat block diagram , derive expression for R_{iF} , R_{OF} G_{mF} for voltage Series Negative Feedback Amplifier.Give significance of the above mentioned parameters. [10M]

Ans :i) In the voltage series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as shunt-driven series-fed feedback, i.e., a parallel-series circuit.

ii) The following figure shows the block diagram of voltage series feedback, by which it is evident that the feedback circuit is placed in shunt with the output but in series with the input.



iii) As the feedback circuit is connected in shunt with the output, the output impedance is decreased and due to the series connection with the input, the input impedance is increased.Voltage series network feedback is series – shunt feedback.



iv) Voltage series negative feedback amplifier is voltage amplifier having very large input impedance .

From circuit diagram , we know that ,

Vin = Vs – Vf and feedback factor is β = Vf/Vo

v) Voltage is taken in shunt and feedback is in series and hencde it is called as Voltage series feedback circuit.

vi) Derivation for input impedance RiF :

From circuit shown , Vs – Iin.Rs – Iin.Rin – Vf = 0

Vs = Iin.Rs + Iin.Rin + Vf

Vs = Iin.Rs + Iin.Rin + β Vo

But Vo = $\frac{RL}{RL+Ro}$. $Av.Vin$

Vo = AvL . Vin

On solving this we get , Vs = Iin[Rs + Rin(1+ β.AvL)]

Hence , input impedance with feedback is Rif = Ri*(1+A*β)

vii) Derivation for output impedance RoF :

Av.Rin – Io.Ro – Vo =0

∴ Av.Rin – Io.Ro = Vo

∴ Vo =Av.$\frac{Vs-Vf}{Ri+Rs}$.$Ri - Io.Ro$

Vo = Avs.(Vs-Vf) – Io.Ro

∴ Vo = Avs.Vs – Avs.Vo. β – Io.Ro

∴ Vo = $\frac{Avs}{1+\beta.Avs}$.$Vs - Io\frac{Ro}{1+Avs.\beta}$

But we know that ,

Vo = AvF.Vf – Io.RoF

On comparing we will get output impedance with feedback i.e

∴ Rof=Ro/(1+A*β)

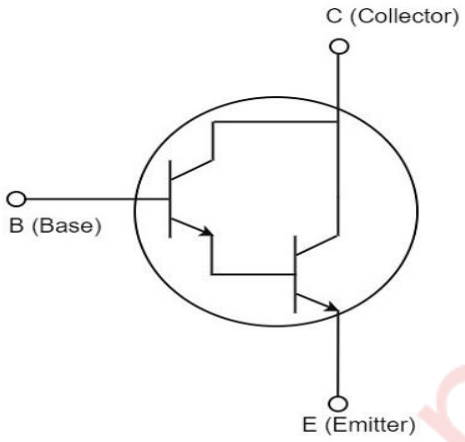
viii) Gain with feedback : From above two derivation of input and output imepdance we get to know that the gain of voltage series network is given by ,

AvF = $\frac{Av}{1+Av.\beta}$

ix) In voltage series feedback circuit , stability of transfer gain improves Av,frequency and pahse distortion decreases , noise and non linear distortion decreses, bandwidth increases , input impedance and increases whereas output impedance decreases.

b) Write a short note on : Darlington pair amplifier. [10M]

Ans : i) Darlington pair, contains of two BJTs that are connected to deliver a high current gain from a low base current. In this transistor, the emitter of the i/p transistor is connected to the o/p of the base of the transistor and the collectors of the transistor are wired together.



ii) So, the i/p transistor amplifies the current even further amplifies by the o/p transistor. Darlington transistors are classified into different types by Power Dissipation, Max CE Voltage, Polarity, Min DC Current Gain and type of Packaging.

iii) The common values of max CE voltage are 30V, 60V, 80V & 100V. The max CE voltage of Darlington transistor is 450V and power dissipation can be in the range of 200mW to 250mW.

iv) The following are the important characteristics of Darling ton amplifier.

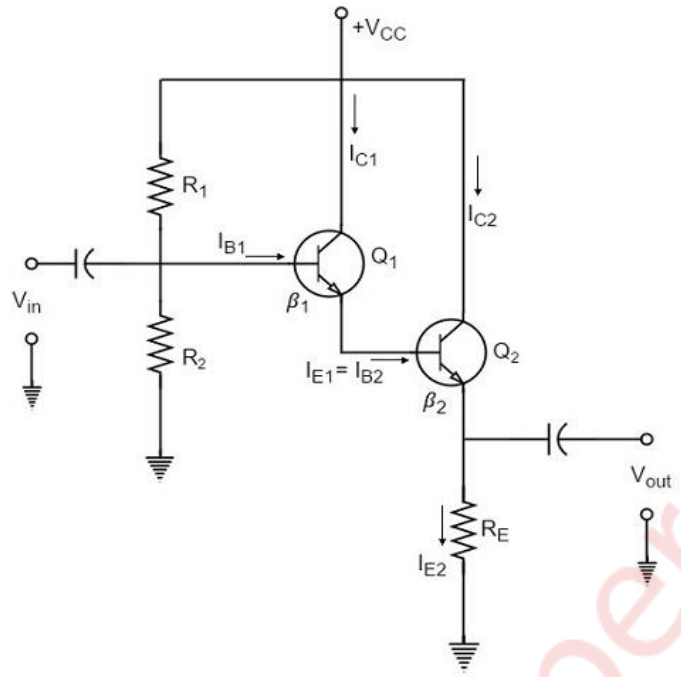
---Extremely high input impedance (MΩ).

---Extremely high current gain (several thousands).

---Extremely low output impedance (a few Ω).

v) The emitter follower circuit which was just discussed lacks to meet the requirements of the circuit current gain (A_i) and the input impedance (Z_i).

vi) In order to achieve some increase in the overall values of circuit current gain and input impedance, two transistors are connected as shown in the following circuit diagram, which is known as Darlington configuration.



$\therefore \quad Ic = Ic1 + Ic2$

$\therefore \quad Ic = \beta1.IB + \beta2.IB2$

vii) But the base current of the transistor Q1 is equal to IE1(emitter current), and emitter of the TR1 transistor is connected to the base terminal of the transistor Q2.

$$IB2 = IE1$$
$$= Ic1 + IB$$
$$= \beta1.IB + IB$$
$$= IB(\beta1 + 1)$$

Substitute this IB2 value in the above equation

$\therefore \quad Ic = \beta1.IB + \beta2.\ IB(\beta1 + 1)$

$\therefore \quad Ic = \beta1.IB + \beta2.\ IB\ \beta1 + \beta2.\ IB$

$\therefore \quad Ic = (\beta1 + (\beta2.\beta1) + \beta2).\ IB$

In the above equation, β1 and β2 are gains of individual transistors.

vii) Here, the overall current gain of the first transistor is multiplied by the second transistor that is specified by β, & a couple of bipolar transistors are combined to form a single Darlington transistor with a very high i/p resistance and value of β.

viii) Darlington Transistor Applications :

This transistor is used in various applications where a high gain is required at a low frequency. Some applications are

---Power Regulators
---Audio Amplifier o/p stages
---Controlling of motors
---Display drivers
---Controlling of Solenoid
---Light and touch sensors.

Q.4 a) Find the necessary condition for oscillations to occur and frequency of oscillations of Colpitts oscillator.Also explain its working. [10M]

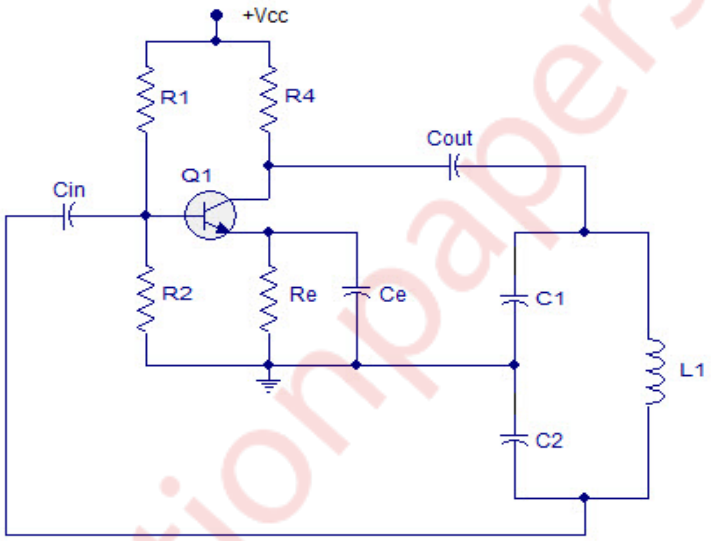
Ans : i) Oscillator is an amplifier with the positive feedback and it converts DC input signal into AC output waveform with certain variable frequency drive and certain shape of output waveform (like sine wave or square wave, etc) by using the positive feedback instead of input signal. Oscillators which utilizes the inductor L and capacitor C in their circuit are called as LC oscillator which is a type of linear oscillator.

ii) It consists of a tank circuit which is an LC resonance sub circuit made of two series capacitors connected in parallel to an inductor and frequency of oscillations can be determined by using the values of these capacitors and inductor of the tank circuit.

iii) This oscillator is almost similar to Hartley oscillator in all aspects; hence, it is termed as electrical dual of Hartley oscillator and is designed for the generation of high frequency sinusoidal oscillations with the radio frequencies typically ranging from 10 KHz to 300MHz. The major difference between these two oscillators is that it uses tapped capacitance, whereas the Hartley oscillator uses tapped inductance.

iv) Every other oscillator circuit which generates sinusoidal waveforms utilizes the LC resonant circuit except a few electronic circuits such RC oscillators, Wien-Robinson oscillator and a few crystal oscillators which don't require additional inductances for this purpose.

v) It can be realized by using gain device such as Bipolar Junction Transistor(BJT), operational amplifier and field effect transistor(FET) as similar in other LC oscillators also. The capacitors C1 & C2 forms potential divider and this tapped capacitance in the tank circuit can be used as the source for feedback and this setup can be used to provide better frequency stability compared to the Hartley oscillator in which tapped inductance is used for feedback setup.



Circuit Diagram of Colpitts Oscillator

vi) Whenever power supply is switched on, the capacitors C1 and C2 shown in the above circuit start charging and after the capacitors get fully charged, the capacitors starts discharging through the inductor L1 in the circuit causing damped harmonic oscillations in the tank circuit.

vii) Thus, an AC voltage is produced across C1 & C2 by the oscillatory current in the tank circuit. While these capacitors get fully discharged, the electrostatic energy stored in the capacitors get transferred in the form of magnetic flux to the inductor and thus inductor gets charged.

viii) Similarly, when the inductor starts discharging, the capacitors start charging again and this process of energy charging and discharging capacitors and inductor continues

causing the generation of oscillations and the frequency of these oscillations can be determined by using the resonant frequency of the tank circuit consisting of inductor and capacitors. This tank circuit is considered as the energy reservoir or energy storage. This is because of frequent energy charging and discharging of the inductor, capacitors that part of LC network forming the tank circuit.

ix) The continuous undamped oscillations can be obtained from the Barkhausen criterion. For sustained oscillations, the total phase shift must be 360deg. or 0deg.. In the above circuit as two capacitors C1 & C2 are center tapped and grounded, the voltage across capacitor C2 (feedback voltage) is 180deg. with the voltage across capacitor C1 (output voltage). The common emitter transistor produces 180deg. phase shift between the input and output voltage. Thus, from the Barkhausen criterion we can get undamped continuous-oscillations.

x) The resonant frequency is given by

$$f_r = \frac{1}{2\pi\sqrt{L1.C}}$$

Where fr is the resonant frequency

C is the equivalent capacitance of series combination of C1 and C2 of the tank circuit

It is given as

$$C = \frac{C1\ .\ C2}{C1 + C2}$$

L1 represents the self inductance of the coil.

xi) Applications of Colpitts Oscillator

---It is used for generation of sinusoidal output signals with very high frequencies.

---The Colpitts oscillator using SAW device can be used as the different type of sensors such as temperature sensor. As the device used in this circuit is highly sensitive to perturbations, it senses directly from its surface.

---It is frequently used for the applications in which very wide range of frequencies are involved.

---Used for applications in which undamped and continuous oscillations are desired for functioning.

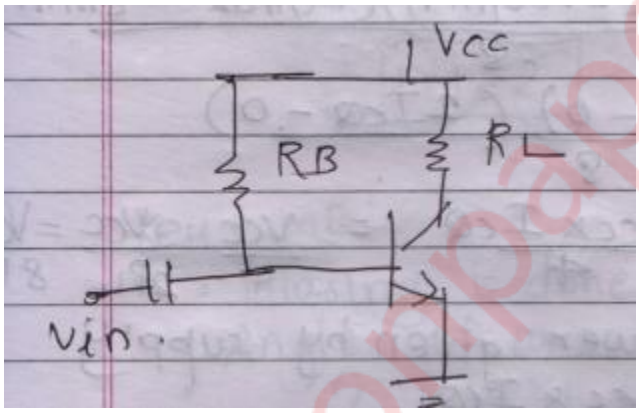
b) Draw a neat diagram of Direct coupled class A amplifier and explain its working.

[10M]

Ans : i) Class A power amplifier is a type of power amplifier where the output transistor is ON full time and the output current flows for the entire cycle of the input wave form.

ii)Class A power amplifier is the simplest of all power amplifier configurations. They have high fidelity and are totally immune to crossover distortion they are not the prime choice because of their poor efficiency.

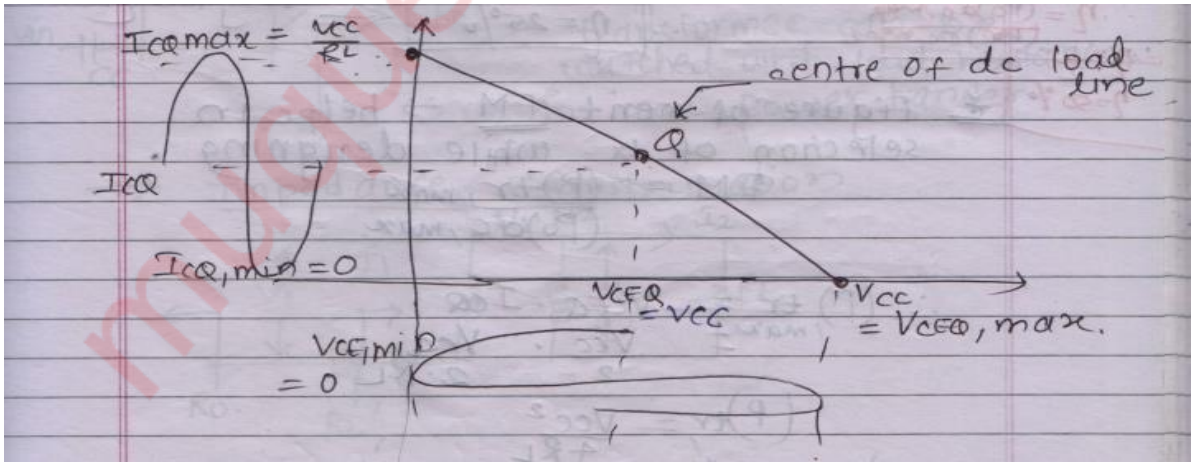
iii) Since the active elements (transistors) are forward biased full time, some current will flow through them even though there is no input signal and this is the main reason for the inefficiency.



iv) In direct coupled amplifier load is directly coupled to collector.

For loadline , apply KVL in output loop, Vcc – I(CQ).RL – V(CEQ) = 0

When V(CEQ)=0 , I(CQ)= Vcc/RL , When I(CQ) = 0 , V(CEQ) = Vcc



v) From the above figure its is clear that the Q-point is placed exactly at the center of the DC load line and the transistor conducts for every point in the input waveform. The theoretical maximum efficiency of a Class A power amplifier is 50%.

vi) In practical scenario, with capacitive coupling and inductive loads (loud speakers), the efficiency can come down as low as 25%. This means 75% of power drawn by the amplifier from the supply line is wasted.

vii) Majority of the power wasted is lost as heat on the active elements (transistor).As a result, even a moderately powered Class A power amplifier require a large power supply and a large heatsink.

viii) Now , Po(ac) = AC power delivered to load

$$\text{Po(ac)}=\frac{\big(V(CEmax)-V(CEmin)\big).\big(I(Cmax)-I(Cmin)\big)}{8} = \frac{Vcc \times I(CQ)}{4} = \frac{Vcc^2}{8RL}$$

Pin (DC) is DC input power given to input .

Pin(DC) = Vcc × I(CQ)

Efficiency is given by , $\eta = \frac{Po(ac)}{Pin(DC)} = \frac{\frac{Vcc^2}{8RL}}{Vcc \times I(CQ)} = \frac{1}{4}$

Hence efficiency is 25 % .

ix) Advantages : ---Class A design is the simplest.

--- High fidelity because input signal will be exactly reproduced at the output.

--- Since the active device is on full time, no time is required for the turn on and this improves high frequency response.

--- Since the active device conducts for the entire cycle of the input signal, there will be no cross over distortion.

--- Single ended configuration can be practically realized in Class A amplifier. Single ended means only one active device (transistor) in the output stage.

x) Disadvantages :

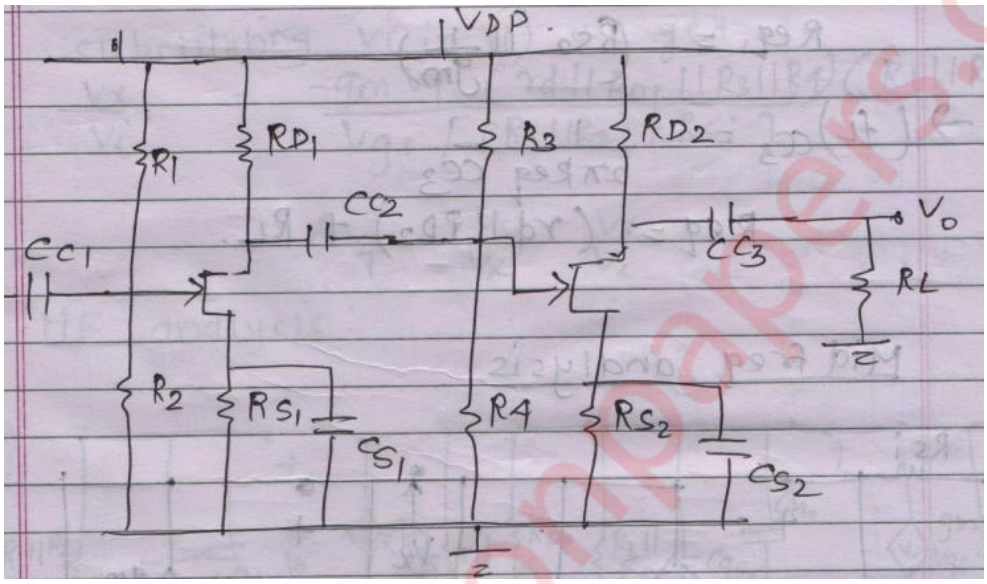
---Main disadvantage is poor efficiency.

---Steps for improving efficiency like transformer coupling etc affects the frequency response.

---Powerful Class A power amplifiers are costly and bulky due to the large power supply and heatsink.

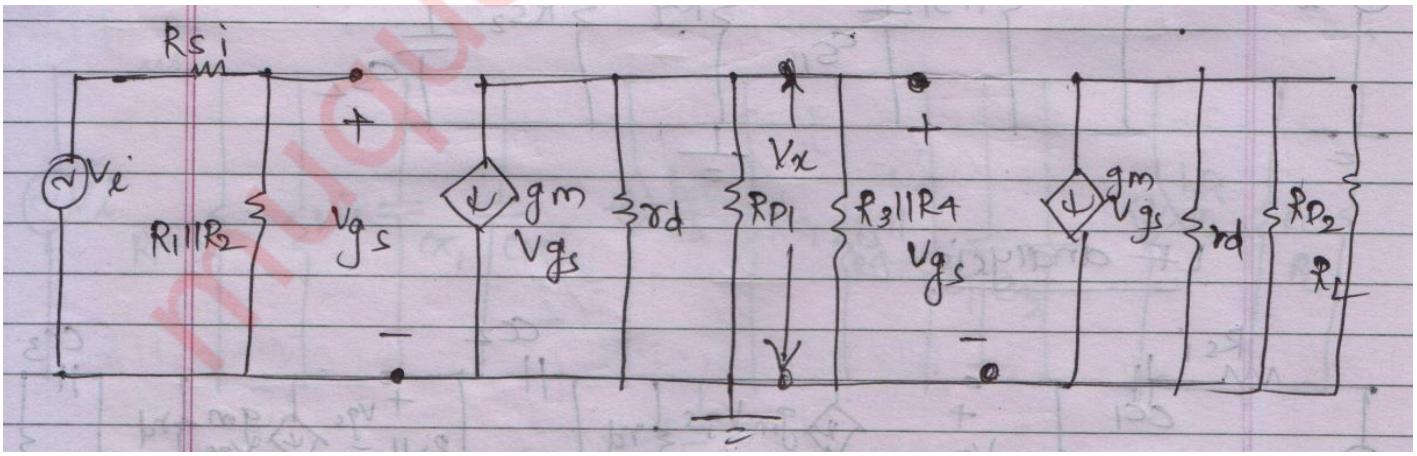
Q.5 a) Determine input impedance , output impedance , voltage gain and current gain for the given cascaded amplifier as shown in the figure below : [10M]

Ans :



i) The given circuit is two stage common source amplifier i.e CS-CS amplifier which is RC coupled.

ii) In order to get voltage gain,current gain of given amplifier analysis of mid frequency is required.And mid frequency analysis is given by ,



ii) Derivation for voltage gain : We know that gain is ratio of output voltage to the input voltage , therefore ,

$$Av = \frac{Vo}{Vi} = \frac{Vo}{Vx}\frac{Vx}{Vi}$$

$$\frac{Vo}{Vx} = \frac{-gm.Vgs(rd||RD2||RL)}{Vgs}$$

$$\frac{Vo}{Vx} = -gm.(rd||RD2||RL)$$

$$Now\ , \frac{Vx}{Vi} = \frac{-gm.Vgs(rd||RD1||R3||R4)}{Vi}$$

But Voltage Vgs is given by , $Vgs = Vi$

$$\frac{Vx}{Vi} = \frac{-gm.Vgs(rd||RD1||R3||R4)}{Vgs}$$

$$\frac{Vx}{Vi} = -gm.(rd||RD1||R3||R4)$$

$$Therefore\ , voltage\ gain\ is\ given\ by\ ,$$

$$Av = gm^2\ .(rd||RD2||RL)\ .(rd||RD1||R3||R4)$$

iii) Derivation for input and output impedance :

In mid frequency analysis, gate to source terminal acts as open circuit and hence input impedance is given by , Rin = R1||R2 and output impedance is given by Ro=RD2||rd.

b) Draw circuit diagram of cascode amplifier and explain in detail. [10M]

Ans : i) Cascode amplifier is the two stage amplifier in which common emitter stage is connected to common base stage. The input signal is applied at Q1 i.e at common emitter stage and output is obtained at Q2.

ii)A common-base configuration is not subject to the Miller effect because the grounded base shields the collector signal from being fed back to the emitter input. Thus, a C-B amplifier has better high frequency response. The way to reduce the common-emitter gain is to reduce the load resistance.

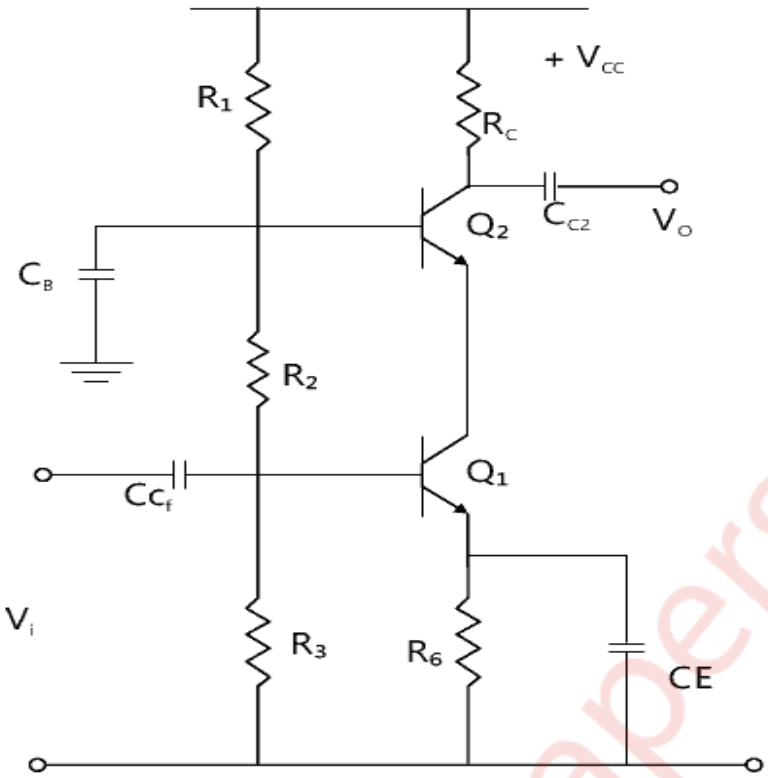
iii)The gain of a C-E amplifier is approximately Rc/R e. The collector load Rc is the resistance of the emitter of the C-B stage loading the C-E stage. CE gain amplifier gain is approximately Av = Rc/Re=1. This Miller capacitance is Cmiller = Ccbo(1-Av) = Ccbo (1-(-1)= 2 Ccbo. Cascode amplifier 15 Ccbo (1-(-1)= 2 Ccbo. We now have a moderately high input impedance C-E stage without suffering the Miller effect, but no C-E stage voltage gain. The C-B stage provides a high voltage gain.

iv)The total current gain of cascode is β as current gain of the C-E stage is 1 for the C-B is β. A cascode amplifier has a high gain, moderately high input impedance, a high output impedance, and a high bandwidth.

v)The cascode is a two-stage amplifier composed of a single transconductance amplifier (usually a common source/emitter stage) followed by a current follower (usually a common gate/base stage).

vi) Compared to a single amplifier stage, this combination may have one or more of the following advantages: higher input-output isolation, higher input impedance, higher output impedance, higher gain or higher bandwidth. In modern circuits, the cascode is often constructed from two transistors (BJTs or FETs), with one operating as a common emitter/source and the other as a common base/gate.

vii)The cascode improves input-output isolation (or reverse transmission) as there is less direct coupling from the output to input. This greatly reduces the Miller multiplication of stray coupling capacitance between input and output and thus contributes to a much higher bandwidth.



CASCODE amplifier

viii) The advantage of the cascode configuration stems from the placement of an upper transistor as the load of the input transistor's output terminal (collector / drain). This upper transistor is referred to as the cascode device. Because at high frequencies the cascode transistor's base/gate is effectively grounded by DC voltage source VBias, the cascode device's emitter / source voltage (and therefore the lower input transistor's collector / drain) is held at a more constant voltage during operation. In other words, the cascode device exhibits a low input resistance to the lower transistor, making the voltage gain seen at the collector / drain of the lower device very small, which dramatically reduces the Miller feedback capacitance from the lower transistor's collector to base or drain to gate.

ix)This loss of voltage gain is recovered by the cascode transistor. Thus, the cascode transistor permits the lower common emitter / source stage to operate with minimum negative (Miller) feedback, improving the bandwidth of the overall amplifier.

x) The base or gate of the cascode device is electrically AC grounded, so charge and discharge of stray capacitance Ccb or Cdg between collector and base or drain and gate is simply through RL the output load, and the frequency response is affected only for

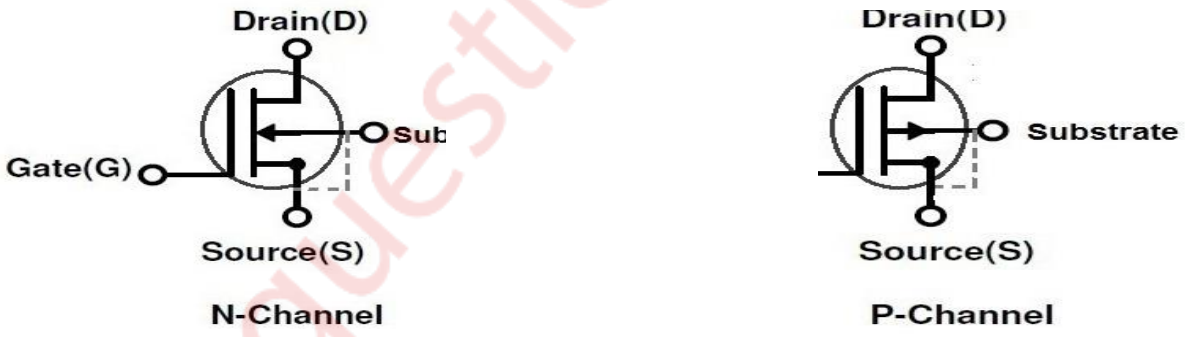
frequencies above the associated RC time constant: In the case of a FET device t = Cdg RD||Rout, a rather high frequency because Cdg is small. That is, the upper FET gate does not suffer from Miller multiplication of Cdg.

xi) If the cascode device stage were operated alone using its emitter or source as input node (i.e. common base/gate configuration), it would have good voltage gain and wide bandwidth. However, its low input impedance would limit its usefulness to very low impedance voltage drivers. Adding the lower common emitter/source stage results in an increased input impedance, allowing the cascode stage to be driven by a higher impedance source.

xii) If one were to replace the upper device with a typical resistive load, and take the output from the input transistor's collector or drain the common emitter/source configuration would offer the same input impedance as the cascode configuration, but the cascode configuration would offer a potentially greater gain and much greater bandwidth.

Q.6 a) State and explain different types of biasing techniques for depletion type MOSFET. [8M]

Ans : i) The depletion type MOSFET transistor is equivalent to a “normally closed” switch. The depletion type of transistors requires gate – source voltage (V_{GS}) to switch OFF the device.



ii) The symbols for depletion mode of MOSFETs in both N-channel and P-channel types are shown above. In the above symbols we can observe that the fourth terminal substrate is connected to the ground, but in discrete MOSFETs it is connected to source terminal.

iii) The continuous thick line connected between the drain and source terminal represents the depletion type. The arrow symbol indicates the type of channel, such as

N-channel or P-channel. In this type of MOSFETs a thin layer of silicon is deposited below the gate terminal. The depletion mode MOSFET transistors are generally ON at zero gate-source voltage (V_{GS}).

iv)The conductivity of the channel in depletion MOSFETs is less compared to the enhancement type of MOSFETs.

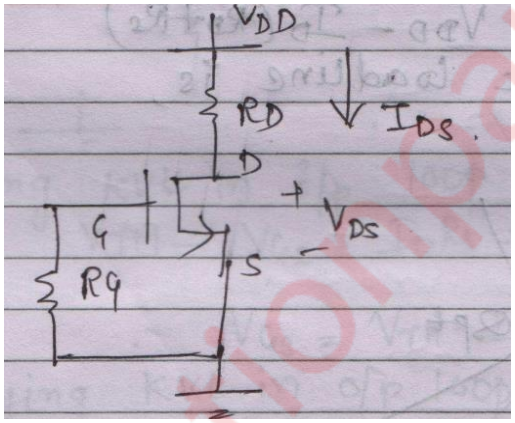
v) The various biasing circuits for D- MOSFET are :

-- Zero Biasd Circuit

-- Self Biasd

-- Voltage Divider Biased

vi) Zero Bias : In this biasing technique , Vg = 0 as Ig = 0 and V(GS) = 0V and V(DS)=V(DD)-ID.RD



vii) Self Biased :

Apply KVL in I/P loop,

-V(GS)-ID.RS = 0

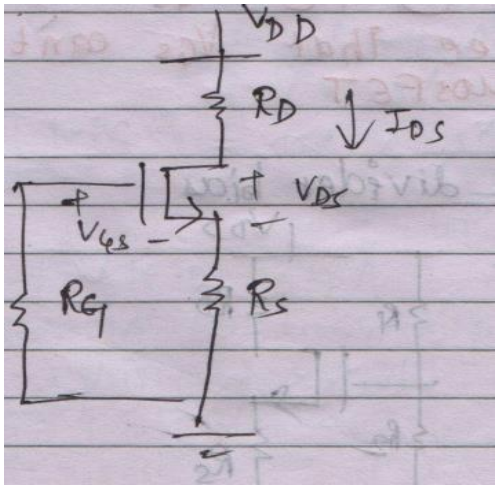
-V(GS) = ID.RS

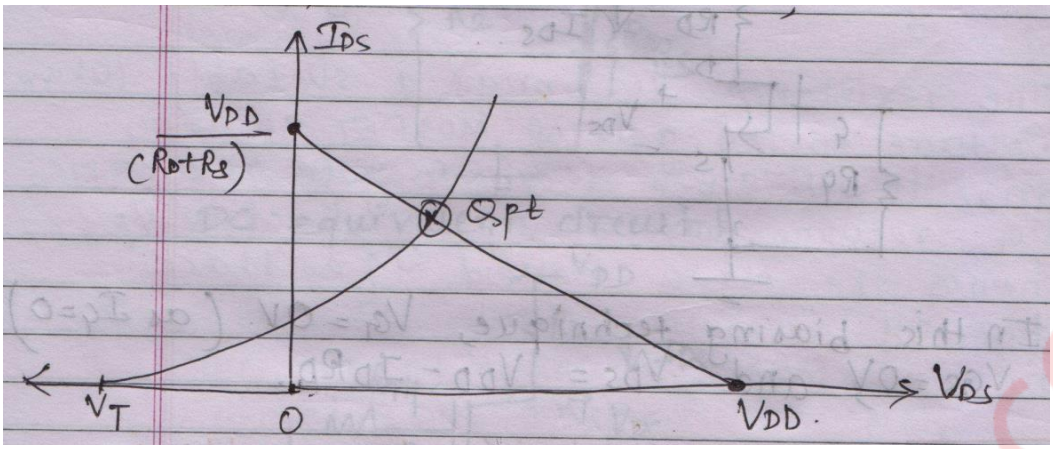
Apply KVL in O/P loop ,

V(DD)-ID.RD-V(DS)-ID.RS = 0

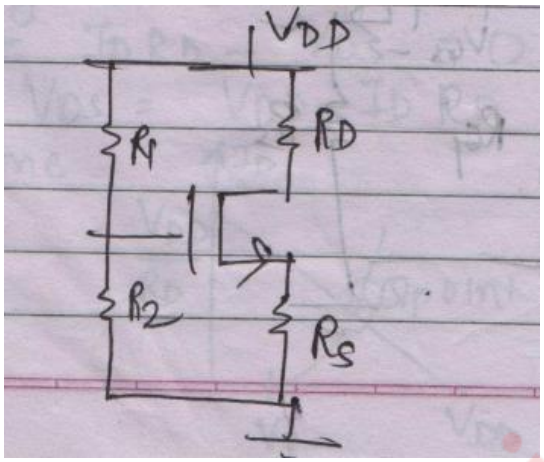
V(DD)-ID.RD-ID.RS = V(DS)

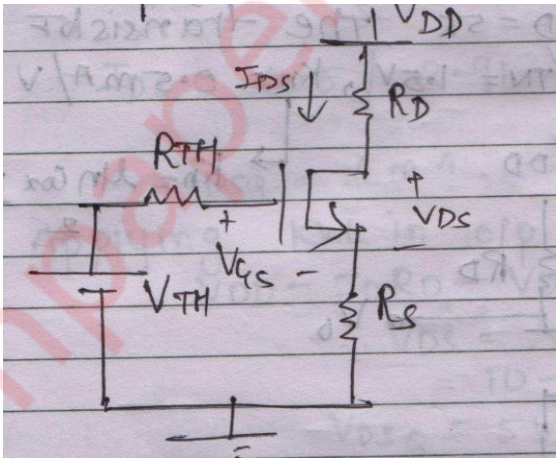
DC loadline is shown below.





viii) Voltage divider biased : Voltage divider bias circuit with its Thevenins equivalent circuit is :





V(TH)= $\frac{R2}{R1+R2}.Vdd$ & R(TH)= R1 || R2

Applying KVL in i/p loop ,

V(TH) – V(GS) – ID.RS = 0

∴ V(TH) – ID.RS = V(GS)

Applying KVL in o/p loop,

Vdd – ID.RD –V(DS) –ID.RS = 0

∴ Vdd – ID.RD –ID.RS = V(DS)

b) Explain the concept of heat sink in detail required for power amplifiers.

A silicon power transistor is operated with a heat sink with $Q_{SA} = 1.2° \frac{C}{W}$. the transistor is rated for 120W at 25°C and has $Q_{JC} = 0.5° \frac{C}{W}$.The mounting insulation has $Q_{CS} = 0.5° \frac{C}{W}$. What maximum power can be dissipated if the ambient temperature is 40 °C and $T_{J(max)}$200 °C . [7M]

Ans : [A] Heat sink for power amplifier :

i) Heat sinks are used for power transistors as the power dissipated at their collector junction is large. If heat dissipation is not done, this will cause large increases in junction temperature. In a transistor, the collector to base junction temperature (temperature of surrounding air) rises or because of self-heating.

ii) The self-heating is due to the power dissipated at collector junction This power dissipation at junction causes the junction temperature to rise, and this in turn increases the collector current which causes further increase in power dissipation. If the phenomenon continues then it may result in permanent damage of the transistor. This is known as thermal runaway.

iii)In power transistor or large signal transistors, the power to be dissipated at the collector causes junction temperature to rise to a high level. It is possible to increase the power handling capacity of the transistor if a device that can cause rapid conduction of heat away from the junction is used. Such a device is called a heat sink. A heat sink is a mechanical device. It is connected to the case of the semiconductor device. So it is providing a path for the heat transfer. The heat flows through the heat sink and is radiated to surrounding air. If a heat sink is not used then all the heat has to he transferred from a transistor case to surrounding air causing case temperature to increase. If the power handled by the transistor is higher, then the case temperature will he higher.

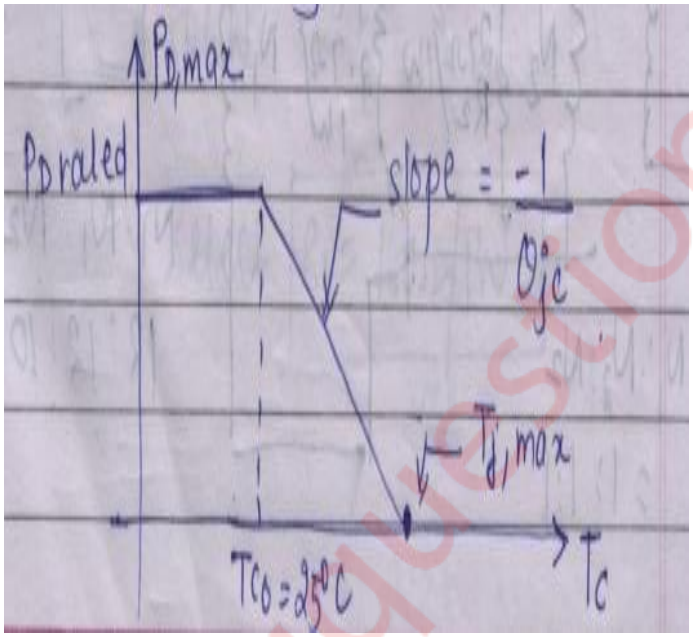
iv) The temperature of the two types of power transistor is Germanium: 100°C to 110°C Silicon : 150°C to 200°C Heat sinks increase the power rating (ie. power handling capacity) of a transistor by getting rid of the heat developed quickly.

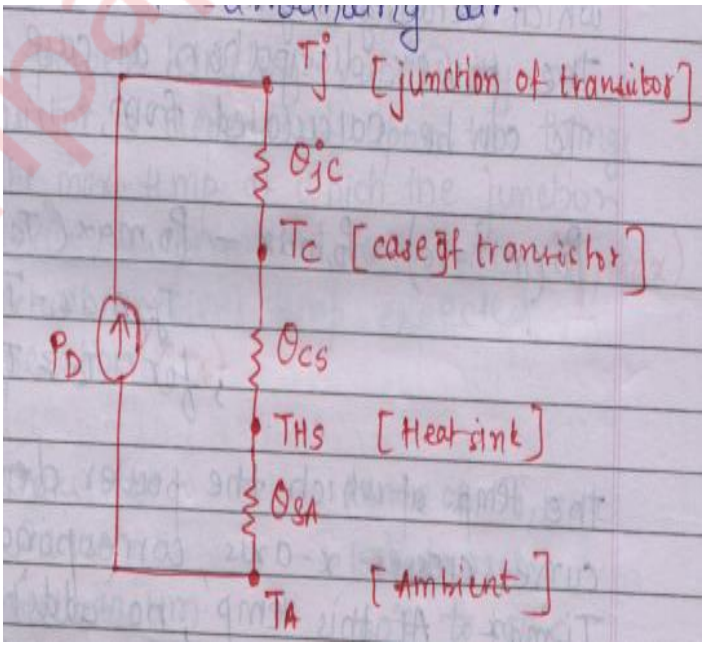
v) It is in the form of a sheet of metal. Since the power dissipation within a transistor is mainly due to power dissipated at collector junction, the collector (connected to the case of the transistor) is bolted on to metal sheet for faster radiation of heat.

vi) Sometimes the transistor is connected to a large heat sink with fins causing more efficient removal of heat from the transistor. When heat flows out of a transistor, it passes through the case transistor and into the heat sink, which then radiates the heat into the surrounding air.

viii) The temperature of the transistor case T will be slightly higher than the temperature of the heat sink which in turn is slightly higher than the ambient temperature TA. Ambient Temperature: The heat produced at the junction passed through the transistor case (metal or plastic housing) are radiates to the surrounding air. The temperature of this air is known as the ambient temperature.

ix) Power derating curve : A plot of maximum rated power of device versuscase temperature of transistor is called as power derating curve of transistor.





[B] Numerical : Given : $Q_{SA} = 1.2° \frac{C}{W}., Q_{JC} = 0.5° \frac{C}{W}, Q_{CS} = 0.5° \frac{C}{W}$

$T_{J(max)}$ =200 °C , Ta = 40 °C

To Find : Maximum power dissipation for given condition = ?

Solution : We know that , maxium power dissipation is given by ,

Tj(max) = Maximum Temperature at junction of trasnsistor.

Ta = Ambient Temperature

Pd(max) = $\frac{T_{J(max)} - \text{Ta}}{Q_{SA}+Q_{JC}+Q_{CS}} = \frac{200-40}{1.2+0.5+0.5}$

Pd(max) = 72.72 W

c) Calculate frequency of oscillations for Hartley oscillator if L1 = L2 = 1mH and C =0.2 μF. **[5M]**

Ans : Given : L1 = L2 = 1mH , C = 0.2 μF

To Find : Frequency of oscillations for hatley oscillator = f = ?

Formula : $f_r = \frac{1}{2\pi\sqrt{L.C}}$ **L = L1 + L2**

Solution : We know that the frequency of oscillations for Hartley oscillator is ,

$$f = \frac{1}{2\pi\sqrt{(L1+L2).C}}$$

$$\therefore f = \frac{1}{2\pi\sqrt{(1m+1m).(0.2\mu)}}$$

$\therefore f =$ **7.96 KHz**