Paper / Subject Code: 41025 / Computer Organization & Architecture

23/05/2025 SE IT SEM-IV C-SCHEME COA QP CODE: 10085401

MARKS:80 TIME:03 HRS N.B. 1. Question No 1 is compulsory. 2. Solve any **three** questions out of the remaining five questions. 3. Assume suitable data if necessary. 4. Figures to the right indicate marks. Q. 1. Solve any **four** out of five. a. Discuss Six Stage Instruction pipeline with diagram. b. Explain the full adder with a diagram. c. Discuss any five arithmetic instructions of 8086 with examples. d. Convert (-185.120)₁₀ in the IEEE 754 single precision standard format. e. Explain Memory hierarchy with diagram. Q. 2. a) Explain concept of DMA in detail with diagram b) Discuss various cache memory mapping techniques with diagram (10)Q. 3. a) Draw Flowchart of Restoring division technique and divide 11 by 3 using same technique. (10)b) Discuss Various Key Characteristics of Computer memory. (10)Q. 4. a) Explain architecture of 8086 microprocessor with diagram (10)b) Explain Encoder and Decoder with diagram (10)Q. 5. a) Draw flowchart of Booth's algorithm. Using same algorithm perform multiplication of (-12)*(5). (10)b) Explain addressing modes of the 8086 microprocessor with example. (10)

Q. 6. a) Write short note on any two types of Flip Flops

(10)

b)Minimize the following boolean function using K map

$$F(A, B, C, D) = \sum m(0,1, 2, 3, 8, 9, 10, 11,) + \sum d(12, 13)$$
(10)
