## Paper / Subject Code: 41025 / Computer Organization & Architecture

May 28, 2024 02:30 pm - 05:30 pm 1T01234 - S.E. (Information Technology Engineering) (SEM-IV) (Choice Base Credit Grading System) (R- 19) (C Scheme) / 41025 - Computer Organization & Architecture QP CODE: 10055304

Total marks: 80 [Time: 3 Hours] 1. Question No 1 is compulsory. N.B. 2. Solve any **three** questions out of the remaining five questions. 3. Assume suitable data if necessary. 4. Figures to the right indicate marks. Q. 1. Solve any **four** out of five. a. Explain the working of D flip-flop. b. With the help of a diagram, explain Von-Neumann's architecture. c. Convert (- 20.25)<sub>10</sub> in the IEEE 754 single precision floating point standard. d. Describe the six stage instruction pipeline. e. Draw the memory hierarchy and explain the same. Q. 2. a) Draw the flowchart of Booth's Algorithm and multiply (-5) and (6) using the same. (10)(10)b) Explain half subtractor and full subtractor using truth table and circuit diagram. Q. 3. a) Reduce given Boolean expression using K-Map method,  $f(A,B,C,D) = \sum_{i} (0, 1, 2, 4, 5, 7, 8, 10, 11, 13, 15)$ (10)b) Write an assembly language program for an 8086 microprocessor to find the even and odd numbers from the list of given ten, 8 bit binary numbers. (10)Q. 4. a) Explain Set associative cache mapping technique with example (10)b) Describe Flynn's classification in detail. (10)Q. 5. a) Discuss the various characteristics of Memory. (10)b) Explain design of control unit w.r.t. microprogrammed and hardwired approach. (10)Q. 6. a) Explain different addressing modes of 8086 microprocessors with examples. (10)b) Discuss the need of I/O module and explain its various I/O techniques in brief. (10)