1T01234 - S.E.(Information Technology Engineering)(SEM-IV)(Choice Base Credit Grading System)(R- 2020-21)(C Scheme) / 41025 - Computer Organization & Architecture

QP CODE: 10042954 DATE: 19/12/2023

Time: 3 Hours **Max Marks:80**

N.B. 1. Question No 1 is compulsory.
2. Solve any **three** questions out of the remaining five questions.
3. Assume suitable data if necessary.
4. Figures to the right indicate marks.

Q. 1. Solve **any four** out of five. **(4*5=20)**

a. With the help of a diagram, explain Von-Neumann's architecture.

b. Explain the working of SR flip-flop.

c. Convert $(- 28.125)_{10}$ in the IEEE 754 double precision standard.

d. Describe the six stage instruction pipeline.

e. Compare SRAM and DRAM.

Q. 2. a) Draw the flowchart of Booth's Algorithm and multiply (-7) and (6) using the same. **(10)**

b) Explain Multiplexer and Demultiplexer with one example. **(10)**

Q. 3. a) Reduce given Boolean expression using K-Map method.

$f(A,B,C,D) = \sum (0, 2, 3 ,4 ,5, 8, 9, 10, 12, 14, 15)$ **(10)**

b) Write an assembly language program for an 8086 microprocessor to find the largest of given ten, 8 bit binary numbers. **(10)**

Q. 4. a) Compare Direct and Set associative cache mapping techniques in detail. **(10)**

b) Discuss various pipeline hazards with example. **(10)**

Q. 5. a) Discuss the various characteristics of Memory. **(10)**

b) Explain design of control unit w.r.t. microprogrammed and hardwired approach. **(10)**

Q. 6. a) Explain different addressing modes of 8086 microprocessors with examples. **(10)**

b) Discuss the need of DMA and explain its various techniques of data transfer. **(10)**
