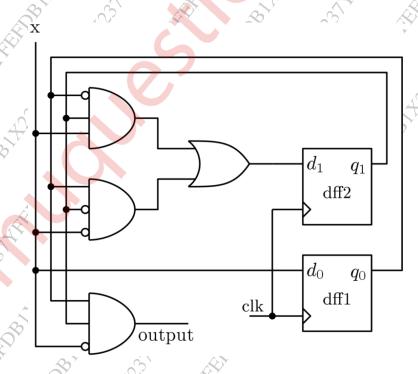
Time: (3 Hours) [Total Marks: 80]

- N.B.: (1) Question No 1 is Compulsory.
 - (2) Attempt any three questions out of the remaining five.
 - (3) Assume suitable data, if required and state it clearly.

1. Attempt any Four

- (a) Write a short note on Moore and Mealy types FSM. [5]
- (b) Compare signal and variable in VHDL with example. [5]
- (c) Write a VHDL code for negative edge triggered <u>J-K</u> flip flop with asynchronous preset and clear.
- (d) Explain the features of VHDL. [5]
- (e) What are the steps involved in digital design with reconfigurable devices? [5]
- 2. (a) Draw a state diagram for a serial adder with minimum number of states.. Write [10] a VHDL code for the same.
 - (b) Analyze the following sequential circuit and hence derive the state table and state diagram. [10]



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3. (a) Design a Mealy sequence detector to detect an overlapping sequence of "0101" [10] using T flip flop.

(b) Write a VHDL code for 8x8 RAM.

1101

[10]

4.	(a)	Present state	Next state		Output	
		A	X=0	X ⇒1	∆ \X=0	X=1
		A S	An	C	1 0	1
		В	A	A F	1 4	1
		C	⊗Ď	E	0	0
		$\sqrt{\mathbf{D}}$	A	G		0 4
		∆ E	В	Ĉ.	0	0
		F	D	Ğ	0	0
	<i>,</i>	$G \Delta V$	B	ॐ C	0	0

State the condition for equivalence of two or more states. Apply state reduction technique to reduce the following state table and hence draw a reduced state diagram.

- (b) Write a VHDL code for 4-bit bidirectional shift register with synchronous reset. [10]
- 5. (a) Write a VHDL code for i) 3:8 decoder ii) 3 bit synchronous UP counter in [10] VHDL.
 - (b) Declare the modules in (Q. 5 a) as components and write a structural code for 8 bit ring counter. (at a time one out of 8 outputs is '1' and this single '1' keeps shifting serially along the 8 outputs.)
- 6. (a) Explain the Booth's Multiplication method and hence write a VHDL code for [10] it.
 - (b) Design a coffee vending machine which accepts 10 rs (T) and 5 rs(F) coins [10] through a, Cost of a cup of coffee is rs. 15. It has two outputs: coffee_out (C) and return_money (R). If extra money is deposited, it returns the balance.

Assume that both the inputs T and F can not be 1 simultaneously.

Clearly state the assumptions if any.

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