T.E. / ELX / Sem-VI / CBCGS / R-19 / 'C' Scheme / Sub:- B.VLSI.D / S.H-2024
Date:- 03/12/2024

(03 Hours) Total Marks (80)

GP. Code:- 10067414

Note:
Question No. 1 is Compulsory.
Answer any three of the remaining questions.
Assume suitable data wherever required

Q1. Solve **any four** of the following **(20)**

a Compare between Full Custom and Semi-custom IC Design Flow.
b Discuss on Static analysis of the Resistive nMOS Inverter.
c Discuss on the Basic gate and MUX Realisation using pass transistor and Transmission gate Logic.
d Implement the function F= $\overline{A + (B + C).(D + E)}$ using static CMOS Logic.
e Write a short note on the VLSI Design Flow

Q2.a Explain CMOS inverter characteristics mentioning all regions of operation. **(10)**

b. Compare Constant field and constant voltage scaling models of MOSFET. State the advantages and limitations of both methods. Show analytically how delay time, power density, and current density are affected in terms of scaling factor in both the types of scaling method **(10)**

Q3.a What are the advantages of CMOS Logic? Design 1 Bit shift Register using CMOS Logic. **(10)**

b. Draw1T DRAM cell and explain its read write and refresh operation **(10)**

Q4.a Explain what is CLA adders and compare it with MODL and Manchester carry chain **(10)**

b. Draw and explain the 4 *4 Barrel Shifter **(10)**

Q5.a State the difference between NAND based and NOR based ROM array. Design a 4*4 NAND based ROM, which stores the following words. Row (0) =0111; Row (1) =1011; Row (2) =1101; Row (3) =1110 **(10)**

b. Compare SRAM with DRAM. Draw 1T DRAM Cell and explain its various operation modes, leakage current and refresh operation. **(10)**

Q6. Write short note on **any four** of the following **(20)**

a C^2MOS
b Sense Amplifier.
c High speed Adder
d Programming techniques for flash memory
e Pseudo NMOS design Style