ELEX SE | Sem-III | Elex. | R-20 | C Scheme | 04.06.2025

Time Duration: 3 Hours **Maximum Marks: 80 Marks**

N.B. : (1) Question No 1 is compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 Attempt any FOUR [20]

a Explain the transfer characteristics of N-channel JFET with a neat sketch & define the term 'transconductance'.

b Compare full-wave bridge type rectifiers & full-wave center-tapped rectifiers.

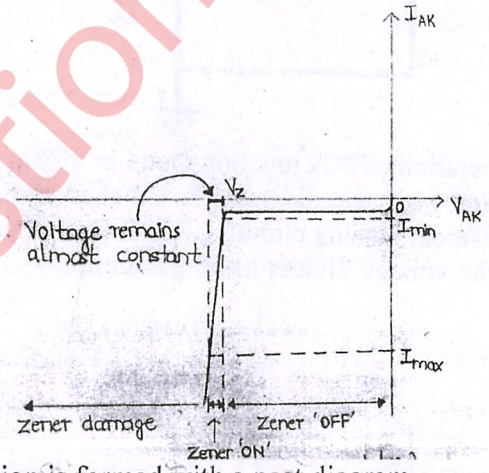
c With neat sketch describes the operation of the inductor (L) filter with appropriate waveforms.

d Explain the concept of DC load line & Q – Point in bipolar junction transistor (BJT).

e Describe any two types of clamper circuits with a neat diagram along with input & output waveforms.

2 a Describe the working or operation of a center-tapped type full wave rectifier with a neat sketch. Draw the output voltage waveforms & mention the expression for DC or average output voltage. [10]

b Identify the electronic circuit as for which the following diode can be used as shown below. Describe its operation for both, varying load resistance with a constant DC supply voltage & a varying DC supply voltage with a constant load resistance. [10]



3 a Explain how a PN junction is formed with a neat diagram. [10]

b Explain with the help of neat diagram construction, working & V-I characteristics of N – channel enhancement MOSFET. [10]

4 a Draw a circuit diagram of common source (CS) E-MOSFET amplifier, derive equation of voltage gain (Av), input resistance (Ri) & output resistance (Ro). [10]

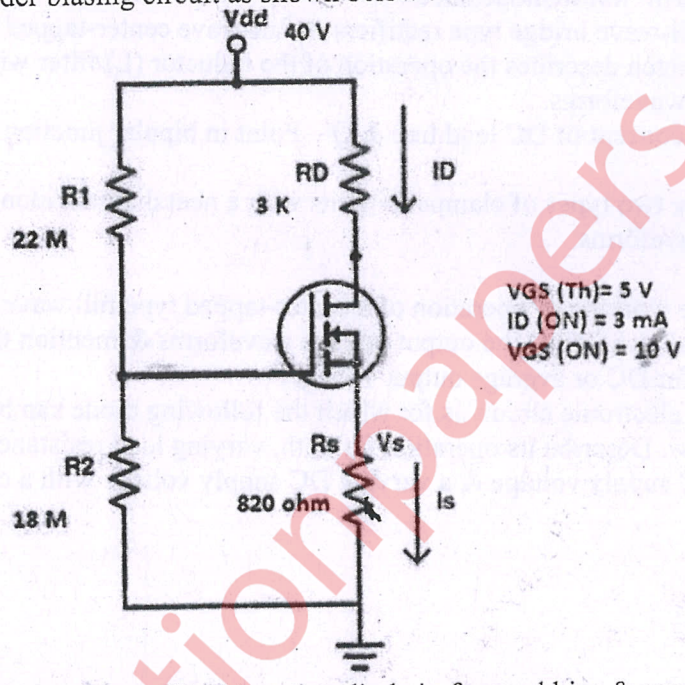
b For small signal amplifier in common emitter (CE) BJT configuration using voltage divider biasing perform small signal (AC) analysis using the hybrid – π model. [10]

Qp code: 82771

Prog. code: 1T01133

5 a With a neat sketch, write a short note on a solar cell describing its structure or construction, working & V-I characteristics. Mention few real-life applications of solar cells [10]

b Calculate the operating point (Q – Point) of the following E-MOSFET using the voltage divider biasing circuit as shown below . [10]



6 a Describe the operation of P-N junction diode in forward bias & reverse bias mode of operation with neat diagrams & V-I characteristics. [10]

b Draw all the different biasing circuits of BJT. Derive the expression of stability factor (SI) for the voltage divider biasing circuit. [10]

****