06.06.2025

SE(ELEX.) | Sem-III | R-20 | C scheme | DLC

(3 Hours) [Total Marks: 80]

Note: (1) Question No. 1 is **Compulsory.**
(2) Attempt any **three** questions out of the remaining **five.**
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

Q.1: (a) Convert T flip flop to D flip flop. (5)

(b) Design a circuit using 2:1 MUX to implement 2-input NAND Gate. (5)

(c) Generate 7-bit even parity Hamming code for data 1101. (5)

(d) Write a Verilog code for Half Subtractor using Gate-level modelling (5)

Q.2 (a) Draw and explain 5-bit Comparator using IC 7485. (10)

(b) Design MOD-8 Synchronous Counter using JK-FF. (10)

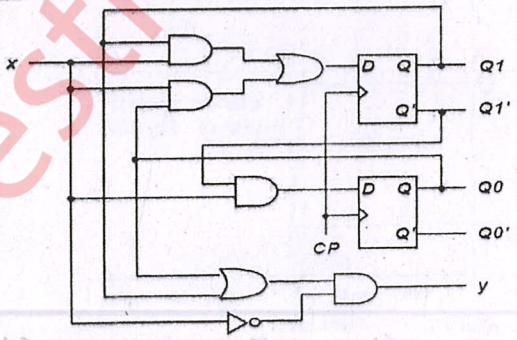
Q.3 (a) Construct 2 input CMOS NAND logic gate and explain. (10)

(b) Design 1- digit BCD Adder using IC 7483. (10)

Q.4 (a) Using K-map reduce given logical function and implement using NAND gates only:

$F(A,B,C,D) = \sum m\,(1,2,3,6,8,9,11,14) + d(0,7,10,15)$ (10)

(b) Analyze the given FSM and obtain the state diagram for the same (10)



Q.5 (a) Implement function F1=∑(4,5,7) and F2 = ∑(3,5,7) using PLA (10)

(b) Draw a circuit diagram of 4-bit SISO shift register and also give its output waveforms. (10)

Q.6 (a) Design Mealy overlapping sequence detector using D-FF to detect 1011. (10)

(b) Write a Verilog code for Full Adder using behavioral modelling style (10)

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qp code 85294

prog. code: IT01133