Duration: 3hrs   **Marks:80**

N.B. : **(1) Question No 1 is Compulsory.**
        (2) Attempt any three questions out of the remaining five.
        (3) All questions carry equal marks.
        (4) Assume suitable data, if required and state it clearly.

1   Attempt any FOUR   [20]

     a   Why is the JFET called as a square law device ?

     b   Compare full-wave bridge type rectifier & full-wave center-tapped rectifiers.

     c   With neat sketch describe operation of the inductor (L) filter with appropriate
         waveforms.

     d   Explain the concept of DC load line & Q – Point in bipolar junction transistor
         (BJT).

     e   Describe two -way clipper circuits with neat diagram & transfer characteristics.

2   a   Describe the working or operation of a bridge type full wave rectifier with a neat   [10]
        sketch. Draw the output voltage waveforms & mention the expression for DC or
        average output voltage (Vdc)

    b   With a neat sketch, explain the Zener diode as a voltage regulator. Describe its   [10]
        operation for both, varying load resistance with a constant DC supply voltage &
        a varying DC supply voltage with a constant load resistance.

3   a   Explain how a PN junction is formed with a neat diagram.   [10]

    b   Explain with the help of neat diagram construction, working & VI characteristics   [10]
        of n channel depletion MOSFET.

4   a   Draw a circuit diagram of common source (CS) E-MOSFET amplifier, derive   [10]
        equation of voltage gain (Av), input resistance (Ri) & output resistance (Ro).

    b   For small signal amplifier in common emitter (CE) BJT configuration using   [10]
        voltage divider biasing perform small signal (AC) analysis using the hybrid – π
        model.

5   a   With a neat sketch, write a short note on solar cell describing its structure or   [10]
        construction, working & V-I characteristics. Mention few real-life applications
        of solar cells

    b   Draw circuit diagram and explain the operation of different biasing circuits used   [10]
        for D-MOSFET.

6   a   Design single stage CE amplifier for $AV \geq 125$, Vorms= 3 V, hfe = 220,   [15]
        hie = 2.7 kΩ, S$\leq$10, $f_L \leq$ 20 Hz, V_{CEsat} = 0.25V, V_{BE} = 0.7 V.

    b   Differentiate between positive and negative clamper.   [05]

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