(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1.	(a)	Design 1-bit comparator circuit using gate.	**(5)**
	(b)	Write Verilog code for 2-input EXOR gate	**(5)**
	(c)	Explain race around condition in JK flipflop. How will you avoid race around condition?	**(5)**
	(d)	Compare CMOS and TTL logic families.	**(5)**
2.	(a)	Design Mod-144 counter using IC7493.	**(10)**
	(b)	Design and Implement sequence detector circuit for 1001 (overlapping sequence) using J-K- flip-flop.	**(10)**
3.	(a)	Design and implement half subtractor using IC74151(Multiplexer)	**(10)**
	(b)	Write Verilog code for 8:1 Multiplexer using structural architecture.	**(10)**
4.	(a)	Design 3-bit Asynchronous counter using JK Flip-Flops.	**(10)**
	(b)	Explain JK flipflop with excitation table, truth table, characteristics equation and state diagram.	**(10)**
5	(a)	Explain in details working of TTL 2 input NAND gate.	**(10)**
	(b)	Draw 4 bit universal shift register using D-Flipflops and explain its operation.	**(10)**
6.	(a)	Explain XC- 4000 FPGA architecture with neat clean diagram.	**(10)**
	(b)	Explain lockout condition in counter with example.	**(10)**