**Paper / Subject Code: 51323 / Digital Logic Circuits** 30|11|2024

SE|EIX|sem-III|CBCGS|R-19-20|C-Scheme|DLC|SH-24

**(3 Hours)** **[Total Marks: 80]**

QP-10066428

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

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|---|---|---|---|
| 1. | (a) | Evaluate the Following Operation in BCD<br>a) $(56)_{10}+(23)_{10}$<br>b) $(48)_{10}+(26)_{10}$ | (5) |
| | (b) | Define A)Noise Margin<br>B)Fan Out | (5) |
| | (c) | Compare Moore and Mealy Circuits | (5) |
| | (d) | Explain core features of Verilog language. | (5) |
| 2. | (a) | Design and Implement Full subtractor circuit using IC74151(Multiplexer) | (10) |
| | (b) | Design and Implement sequence detector circuit for 1011 (non overlapping sequence) using JK flip-flop. | (10) |
| 3. | (a) | Design Mod-100 counter using IC7490 | (10) |
| | (b) | Write Verilog code for Full adder. | (10) |
| 4. | (a) | Design Mod 10 Asynchronous counter using T Flip-Flop. | (10) |
| | (b) | Design Mod-10 counter using IC 74163 | (10) |
| 5 | (a) | Explain the interfacing of a TTL gate driving CMOS gates and vice versa | (10) |
| | (b) | Draw a neat circuit diagram of four bit Twisted Ring Counter with initial state 0000 and relevant output waveforms. | (10) |
| 6. | (a) | Convert the following<br>a)Convert D Flip-Flop into T Flip-Flop b)JK flip-flop to D flip-flop | (10) |
| | (b) | Explain XC 9500 CPLD architecture with neat clean diagram. | (10) |

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