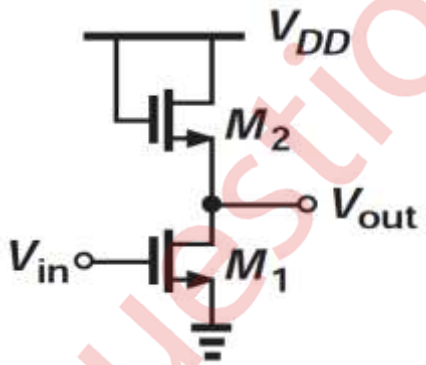
Time: - 3 hrs. **Maximum Marks: - 80**

N. B.

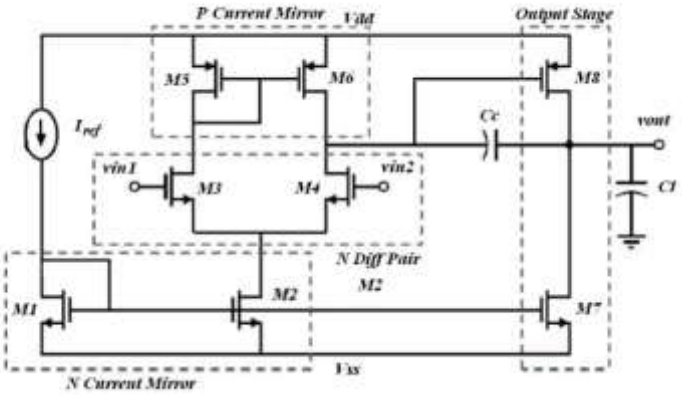
1. Q.1 is compulsory.
2. Answer any **three** out of the remaining five questions.
3. Figures to the right indicate marks.
4. Answer to the questions should be grouped and written together.

Q1.	Solve **any four** out of five	**5**
a.	What is the drawback in Current Mirror circuit? How to overcome it?	
b.	Why do we use frequency compensation in two stage op-amp? Draw the frequency response of compensated two stage op-amp.	**5**
c.	Define the term Resolution of DAC. Find the Resolution of DAC if the output voltage is desired to change in 10 milli-volt increment while using V_{REF}=5V.	**5**
d.	For a 3-bit ADC with V_{REF}=5V, Calculate the value of 1LSB Voltage and value of $V_{STAIRCASE}$ For binary output 001,010,101 and 111.	**5**
e.	Explain different types of noise in MOSFET and thereby draw its equivalent noise circuit.	**5**
Q2 a.	Draw and explain the working of Cyclic DAC give its merits and demerits.	**10**
b.		**10**

Identify the given circuit. Draw its small signal model and derive the expression for V_{IN}/V_{OUT} and output voltage range.

Q3		
a	Derive the expression for Input referred Noise of CG Amplifier with Passive load.	**10**
b	Draw and explain the working of Temperature Independent Band gap Reference voltage source.	**10**

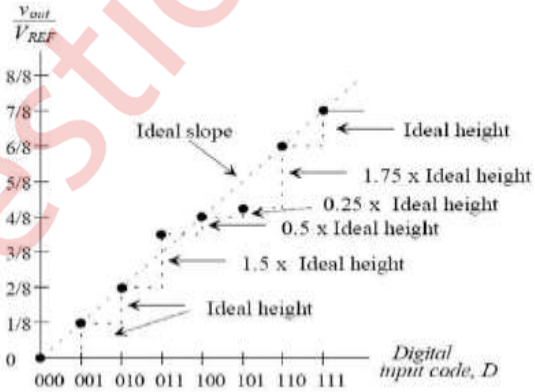
Q4 **20**



Design the given 2 stage operational amplifier for the given specifications.
Phase margin of 60 degree and channel Length =1um
Av > 3500v/v, VDD = 2.5V, V_{SS}=-2.5V, Gain Bandwidth = 6MHz
C_L= 15pf, SR. 10 V/µS, V_{OUT} (range) = +2 to -2V,
ICMR = -1.125 V to +2V, Power Dissipation < 2mw
Threshold Voltage (NMOS) = 0.7V
Threshold Voltage (PMOS) = - 0.7V
Channel length modulation index (NMOS) = 0.04 V^{-1}
Channel length modulation index (PMOS) = 0.05 V^{-1}
$\mu_n C_{OX}$ = 110 µA/V^2 and $\mu_p C_{OX}$ = 50 µA/V^2

Q5 a Draw and explain the Flash type ADC for designing of 3-bit ADC how many comparators will require? **10**

b. **10**



With respect to DAC define the term DNL. Determine the DNL for 3-bit non-ideal DAC whose transfer curve is as shown in figure. Take V_{REF}= 5V.

Q6 **Write short notes on (any four)**

a. Advantages of Active load over Passive load. **5**
b. CS Amplifier with triode load. **5**
c. Types of Noise in MOSFET. **5**
d. Explain various issues associated with Mixed Signal Circuit Layout. **5**
e. Successive Approximation method ADC **5**

****