18/11/2024 EXTC SEM-V C SCHEME DVLSI QP CODE: 10065382

Time: 3 Hours **[Time Marks: 80]**

N.B.: (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 Attempt any FOUR **[20]**

a Draw Layout of CMOS inverter using LAMBDA based rule.

b Explain charge sharing problem in dynamic logic and explain how to overcome it.

c For enhancement type NMOS transistor threshold voltage V_T=0.7V, µnCox =40 µA/V2, W = 10µm, L = 5 µm. Calculate I_D if for VGS = 2 , V_{DS}= 2V

d Draw 4 *4 bit OR based array to store the following data in respective memory locations.

Memory address	Data
1000	1001
0100	1101
0010	1010
0001	1101

e Implement 4:1 mux using pass transistor logic.

2 a Consider a CMOS inverter with following parameters: **[10]**
nMOS VTN = 0.6 V Kn =200 µA/V^2 K_R = 2.5
pMOS VTp = -0.7 V µpCox =80 µA/V^2
Calculate noise margin. The power supply voltage is VDD = 3.0 V.

b Explain CMOS fabrication process using P-well process with neat diagrams. **[10]**

3 a Realize the following **[10]**
1. Clocked SR flipflop.
2. Carry of 4-bit CLA adder.

b Explain 3-T DRAM with its read and write operation, using neat and clean diagrams. **[10]**

4 a Realize $\overline{(AB + CD)}$ gate using the following logic style. **[10]**
1. CMOS logic
2. Dynamic logic
3. Pseudo nMOS Logic
4. Domino Logic

b Design a "Serial FIR Filter" using the RTL design process. Draw HLSM, FSM and data path. **[10]**

5 **a** Realize 4-bit adder using ripple carry adder and carry look ahead adder, compare both realizations based on area and speed. **[10]**

b Compare the effect of Full scaling and Constant voltage scaling on Current, Power, power density. State which is more power efficient. **[10]**

6 **a** Realize 2 – input NOR gate using CMOS logic **[10]**

a) Draw layout of realized circuit.

b) Find equivalent CMOS inverter for simultaneously switching of all input. Assume $(\frac{W}{L})p = 15, \quad (\frac{W}{L})n = 10$

b Write a short note on the following. **(Attempt any TWO)** **[10]**

1. Clock distribution scheme
2. short channel effect (anyone)
3. Flash Memory

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