06/06/2025 SE EXTC SEM-III C-SCHME DSD QP CODE: 10083098

(3 Hours) **Total Marks: 80**

N.B. 1. Question No. 1 is **Compulsory**
2. Out of remaining questions, attempt **any three**
3. **Assume** suitable data if required
4. Figures to the right indicate **full marks**

1. Attempt **any four**

(a) Perform subtraction using 2's complement method **[5]**
i) $(68-24)_{10}$ ii) $(44-60)_{10}$

(b) State and prove De-Morgan's theorem **[5]**

(c) Convert the given Boolean expression to minterms $F(A,B,C,D) = Y = ABC + AC$ **[5]**

(d) Define and explain the following terms in case of logic families: **[5]**
Figure of merit, Fan-in and Fan-Out, Current and Voltage parameters, Noise Margin

(e) Write short notes on FPGA and CPLD **[5]**

2. (a) Draw the block diagram of BCD adder using IC 7483 and show with example the **[10]**
addition of two BCD numbers

(b) Develop a mod 6 Synchronous Counter using T F/Fs which counts in the sequence **[10]**
0-1-2-3-4-5-0. Take care of lockout condition

3. (a) Minimize the following SOP using K-Map and implement using universal gates. **[10]**
$F = \sum m (0,2, 6,7,8,9, 10, 11, 12, 13) + d (14, 15)$

(b) Obtain the minimal expression using tabular method **[10]**
$F = \sum m (1,2, 3,5,6,7,8,9, 12, 13,15)$

4 (a) What is shift register? Explain SISO type of shift register with an example **[10]**

(b) Implement a Full adder using PLA **[10]**

5. (a) Draw and explain the working of a 4-bit Johnson counter with timing diagram **[10]**

(b) Sketch and explain the working of a 4-bit Asynchronous down counter using JK flip **[10]**
flop. Sketch each output with reference to clock

6. Solve the following

(a) Give classification of semiconductor memories and explain DRAM in brief **[5]**

(b) Write VHDL code to build a 4:1 Multiplexer **[5]**

(c) Convert J-K-Flip Flop to T-Flip Flop **[5]**

(d) Convert J-K Flip-Flop to D-Flip-Flop **[5]**

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