Time: 3 hour **Max. Marks: 80**

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Q1 is compulsory.
Attempt any three from Q2 to Q6.

Q1 Solve any Four — 5 marks each

A Explain the operation of a semiconductor pn junction diode with the help of VI characteristics.

B Explain Miller's capacitance theorem.

C What is the effect of coupling and bypass capacitors on the frequency response of a single stage amplifier?

D What is crossover distortion in Class B power amplifiers?

E Explain the working of a two transistor constant current source using E-MOSFET.

Q2 — 10 marks each

A Draw the voltage divider biasing circuit for JFET and derive the quiescent point (V_{DSQ},I_{DQ}) equations.

B Draw a small signal equivalent circuit of the given circuit in fig. 1 and derive the expression for voltage gain, input impedance and output impedance.

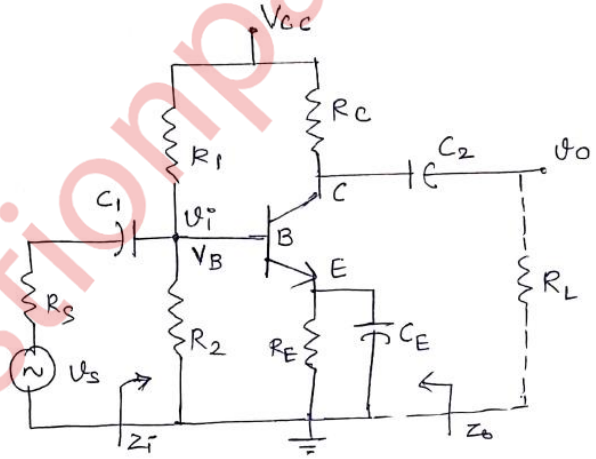

Fig. 1

X525Y1A0C0AX525Y1A0C0AX525Y1A0C0AX525Y1A0C0A

Q3

10 marks each

A For a Class B amplifier providing a 20 V peak signal to a 16 Ω load (speaker) and a power supply of V_{CC} = 30 V, determine the input power, output power and circuit efficiency.

B Calculate low cutoff frequencies due to coupling and bypass capacitors of the circuit given in fig. 2

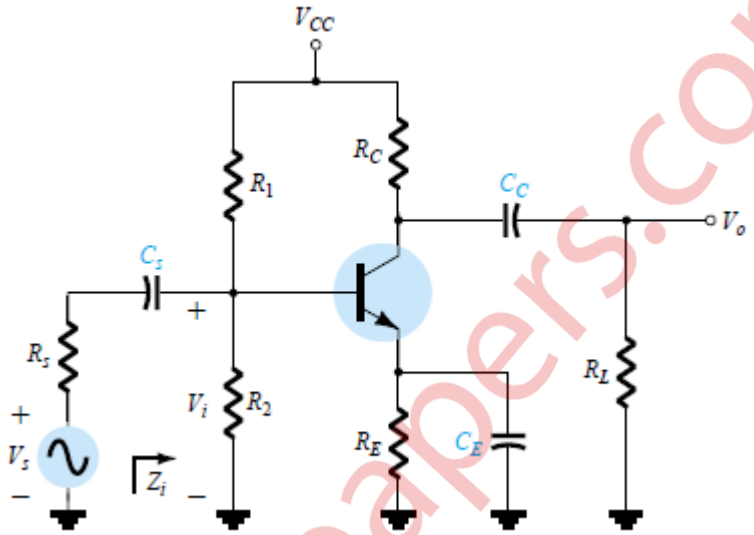

Fig. 2

$C_s = 10\ \mu F, \quad C_E = 20\ \mu F, \quad C_C = 1\ \mu F$

$R_s = 1\ k\Omega, \quad R_1 = 40\ k\Omega, \quad R_2 = 10\ k\Omega, \quad R_E = 2\ k\Omega, \quad R_C = 4\ k\Omega, \quad R_L = 2.2\ k\Omega$

$\beta = 100, \quad r_o = \infty\ \Omega, \quad V_{CC} = 20\ V$

Q4

10 Marks each

A Draw and explain high frequency model for BJT in CE configuration.

B Draw and explain a series fed class A power amplifier with the help of neat diagram and waveforms and derive the expression of power efficiency.

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X525Y1A0C0AX525Y1A0C0AX525Y1A0C0AX525Y1A0C0A

Q5

10 Marks each

A Design a voltage divider bias circuit to operate at the given conditions. Refer Fig. 3

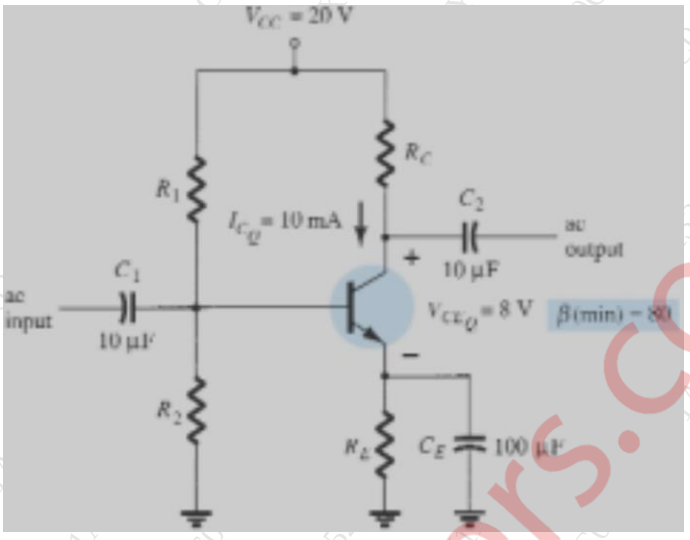

Fig. 3

B Determine the input impedance, output impedance and voltage gain for the given circuit. Refer fig. 4

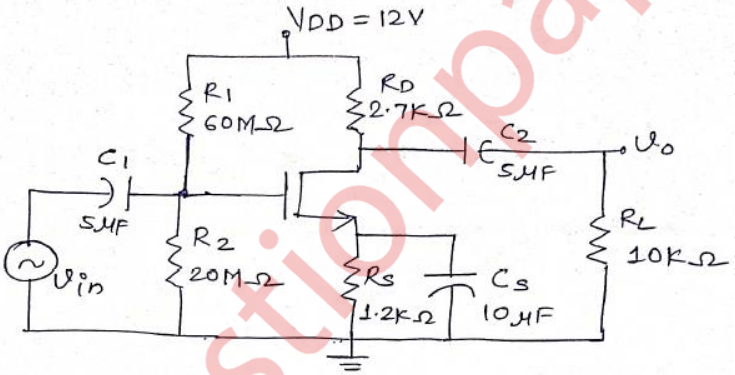

Fig. 4

$K_n' = \mu_n C_{ox} = 100\,\mu A/V^2$, $V_{Tn} = 0.5$ V

$W = 1.8\,\mu m$, $L = 180\,nm$, $\gamma_d = \infty$

$V_{GSQ} = 1.872$ V, $I_{DSQ} = 0.94$ mA

Q6

10 Marks each

A Derive the equation of CMRR for the MOS differential pair amplifier.

B Explain the operation of a MOS differential amplifier with differential mode input signal.

X525Y1A0C0AX525Y1A0C0AX525Y1A0C0AX525Y1A0C0A

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