June 10, 2024 02:30 pm - 05:30 pm 1T01033 - S.E.(Electronics and Telecommunication)(SEM-III)(Choice Base Credit Grading System) (R- 19) (C Scheme) / 51223 - Digital System DesignQP CODE: 10054869

(3 Hours) **Total Marks: 80**

N.B. **1.** Question No. 1 is **Compulsory**
2. Out of remaining questions, attempt **any three**
3. **Assume** suitable data if required
4. Figures to the right indicate **full marks**

1.	**(a)**	Compare SRAM and DRAM	**[5]**
	(b)	Compare Sequential Circuits and Combinational circuits with Suitable Examples	**[5]**
	(c)	State and Prove De Morgan's theorems	**[5]**
	(d)	Design a one-bit magnitude Comparator	**[5]**
2.	**(a)**	Prove that NAND and NOR Gates are universal Gates	**[10]**
	(b)	Perform following	
		i) $25_{10} - 10_{10}$ using two's complement method	**[5]**
		ii) Convert the given decimal number into Hexadecimal 675.625_{10}	**[5]**
3.	**(a)**	Design a 3 bit Binary to Gray code converter and Implement using XOR Gates only.	**[10]**
	(b)	Implement the given function using 16:1 Multiplexer F(A,B,C,D) = ∑m(0, 2, 3, 6, 8, 9, 12,14)	**[10]**
4	**(a)**	Minimize the following expression using Quine McClusky Technique F(A, B, C, D) = ∑m(0, 2, 4, 6, 7, 8, 10, 11, 12, 14, 15)	**[10]**
	(b)	Derive characteristic equation for JKFF	**[5]**
	(c)	Convert JK FF to T FF	**[5]**
5.	**(a)**	Explain a 4-bit asynchronous up counter. Sketch output at each flipflop	**[10]**
	(b)	Write a VHDL program to design a 2:1 Mux	**[5]**
	(c)	Write a VHDL program to design a half adder	**[5]**
6.	**(a)**	Design synchronous mod 8 up counter using JK FF	**[10]**
	(b)	Write a note on CPLDs	**[10]**
