Time: 3 hours **Max. Marks: 80**

N.B.(1) Question No. 1 is compulsory.
(2) Attempt any three questions from remaining five questions.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

Q1. Attempt any four. 20

a. Compare constant voltage scaling and constant field scaling.

b. Realize Boolean function F= $\overline{XY + Z}$ by static CMOS and dynamic CMOS logic style.

c. List advantages of SRAM & DRAM.

d. Draw and explain barrel shifter in brief.

e. Explain briefly about transfer characteristics of CMOS inverter.

Q2. a) Explain design strategy of 6T SRAM cell. 20

b) Design 4:1 Multiplexer using pass transistor logic and CMOS transmission logic.

Q3. a) Explain CMOS inverter characteristics mentioning all regions of operations? 20

b) Explain Pseudo NMOS logic with suitable example.

Q4 a) Draw stick diagram and layout for CMOS based 2 i/p NOR gate. 20

b) Explain the working of resistive load NMOS Inverter. Derive expression for critical voltages.

Q5.a) Write short note on short channel effects. 20

b) Explain carry skip, carry select and carry save high speed adders.

Q6. a) Explain working of CLA and how the speed of the adder can be enhanced? 20

b) Draw and explain clocked SR Latch using static CMOS design style.
