

Time: 3 Hours

Max Marks: 80

- N.B.:** 1) Question No.1 is compulsory.
 2) Solve any three questions from the remaining questions.
 3) Assume suitable data if necessary.

- 1 Solve any Four of the following**
- (a) Implement two input NAND gate using Pseudo NMOS logic? **05**
 (b) Compare semi custom design and full custom design? **05**
 (c) Implement $Y = (A.B) + (C.D)$ using static CMOS logic? **05**
 (d) Explain write operation of 1T DRAM cell? **05**
 (e) State drawbacks of dynamic CMOS logic? **05**
- 2** (a) Explain CMOS inverter characteristics mentioning all regions of operations? **10**
 (b) Implement 4:1 mux using NMOS pass transistor logic? **10**
- 3** (a) Draw 6T SRAM cell and explain it's read and write operation? **10**
 (b) Implement D flip-flop using Static CMOS. What are other design methods for it? **10**
- 4** (a) Draw stick diagram of 2 input NOR gate and draw it's layout in graph paper with suitable design rules? **10**
 (b) Explain Carry Look Ahead adder and it's advantages **10**
- 5** (a) Explain 4*4 Array Multiplier and its operation. **10**
 (b) State techniques of scaling methods and demonstrate effect of scaling method in any 5 CMOS parameters. **10**
- 6 Write short notes on following: (Any Four) 20**
- (a) Power dissipation in CMOS
 (b) Dynamic: C²MOS
 (c) Flash Memory
 (d) Carry Skip Adder
 (e) 4*4 Barrel Shifter
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