[Time: 3 Hours] **[Total Marks: 80]**

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. Attempt Any Four

	(a)	What is instruction cycle of processor?	(5)
	(b)	Define Premptive and Non-Preemptive scheduling.	(5)
	(c)	Compare CPU and GPU	(5)
	(d)	Define CPI, clock speed and MIPS.	(5)
	(e)	What is necessity of cache memory?	(5)
2.	(a)	Expalin Flynn's Classification in detail.	(10)
	(b)	Describe File organization and access.	(10)
3.	(a)	List the difference between deadlock avoidance and Deadlock prevention. Explain one deadlock prevention method.	(10)
	(b)	Explain Multicore processor Architecture.	(10)
4.	(a)	Explain various pipeline hazards. Explain the performance metrics for instruction pipelines	(10)
	(b)	Explain in detail Hardwired control Unit. Discuss any one method to implement it.	(10)
5.	(a)	Explain FIFO page replacement algorithm. Find out number of page faults for the following string using FIFO method with 3 page frames. 4,7,6,1,7,6,1,2,7,2	(10)
	(b)	For the given FCFS scheduling calculate average waiting time and average turnaround time	(10)

Process	Arrival Time	Burst Time
P1	2	2
P2	0	1
P3	2	3
P4	3	5
P5	4	5

6.	(a)	Describe Register organization in CPU.	(10)
	(b)	Compare RISC and CISC architectures.	(10)