ECS-V-CBCG
24/11/22

Time: 3 Hours **Marks: 80**

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. Attempt any FOUR (20)

a) Define MIPS, CPI and MFLOPS.
b) Why does a superscalar processor use dynamic branch prediction? Justify.
c) Draw and explain a typical Instruction Cycle in a processor.
d) Compare CPU and GPU.
e) Why is there a need for communication between two processes? Also write techniques to implement IPC.

2. (a) Compare RISC and CISC architectures. (10)
(b) Explain Pre-emptive and Non-pre-emptive scheduling. Give an example of each type. (10)

3. (a) Explain FIFO page replacement algorithm. Find out Miss ratio, Hit ratio for the following string using FIFO method. (10)
(Consider page frame size = 3)
4 , 7, 6, 1, 7, 6, 1, 2, 7, 2
(b) Explain various pipeline hazards. Explain the performance metrics for instruction pipelines. (10)

4. (a) Explain FCFS scheduling. For the given FCFS scheduling, calculate the average waiting time and average turnaround time. (10)

Process Id	Arrival Time	Burst Time
P1	0	2
P2	3	1
P3	5	6

(b) Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find the number of bits in tag. (10)

5 (a) Describe File organization and access. (10)
(b) Explain in detail Hardwired control unit. Discuss any one method to implement it. (10)

6. (a) List the difference between deadlock avoidance and prevention? Explain one deadlock prevention method. (10)
(b) Explain Multi-core processor architecture. (10)

****