Duration: 3hrs **[Max Marks:80]**

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 Attempt any **FOUR.**

a Write a note on binary codes. [05]

b Draw the block diagram of each and compare Moore machine and Mealy machine. [05]

c Implement the following function using 4:1 multiplexer. [05]

$$f(A, B, C) = \bar{A}BC + A\bar{B}C$$

d Write a Verilog code for full adder. [05]

e Convert T flipflop to D flipflop. [05]

2 a Design a finite state machine of Mealy type that receives data bits serially at the serial input port S. The output Z which is normally Low, should become High for one clock pulse when the machine detects 1-1-1-0 sequence at S. Clearly mention the assumptions. [10]

b Draw a block diagram of BCD adder using IC 7483 and explain the working. [10]

3 a Explain CPLD Architecture with neat block diagram. [10]

b Design MOD 60 counter using any MSI counter ICs and if required minimum number of suitable gates. Explain the design. [10]

4 a i) Explain the working of 3 bit asynchronous counter using flipflops. [07]
ii) Compare its performance with a synchronous counter. [03]

b Write a Verilog code to describe a 3: 8 decoder with active low enable. [10]

5 a Explain the working of i) CMOS NAND ii) CMOS NOR gates with the help of neat circuit diagrams. [10]

b i) Explain the structural difference between PAL and PLA. [05]
ii) Implement the following functions using suitable PAL. [05]

$$f_1 = XY + X\bar{Z}$$

$$f_2 = XY' + YZ + X\bar{Z}$$

6 Write a short note on : [07]
i) State reduction and state assignment in state machine design. [06]
ii) 8 bit Comparator using ICs 7485.
iii) Modelling styles in Verilog. [07]

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X126Y746E6BX126Y746E6BX126Y746E6BX126Y746E6B