SE | ECS | SEM-III | R-19 | SH-2024 Date:- 30/11/24

Q.P. code: 66432

Paper / Subject Code: 51123 / Digital Electronics

(3 Hours) **[Total Marks: 80]**

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

Q1 **Solve any four**

(a) Perform the following operations by using 2's complement method, **(5)**
i) 46-23 ii) -46-25

(b) Using two 74151s, design a 16 line multiplexer controlled by four data select control inputs. **(5)**

(c) Describe the operation of 2 bit synchronous binary counter. **(5)**

(d) Design divide by 4 counter using 7490. **(5)**

(e) Write a code in VHDL to implement 2:1 MUX **(5)**

Q2 **(a)** Simplify the following Boolean expressions **(10)**
i) $Y=\sum m(1,3,7,11,15)+d(0,2,5)$
ii) $Y=\prod M(4,5,6,7,8,12).d(1,2,3,9,11,14)$
Minimize the following Boolean functions,
i) $Y(A,B,C,D)=\sum m(1,3,5,8,9,11,15)+d(2,13)$
ii) $Y(A,B,C,D)=\prod M(1,2,3,8,9,10,11,14).d(7,15)$

(b) Discuss basic comparator operation. Draw the diagram and explain the working of a binary comparator for comparing two 4 bit binary strings. **(10)**

Q3 **(a)** What is the difference between programmable logic array (PLA) and programmable array logic (PAL)? Explain PAL in details. **(10)**

(b) Describe a n bit binary ripple-carry adder showing typical carry propagation delays. **(10)**

Q4 **(a)** Convert, **(10)**
i) T flip flop into D flip flop
ii) D flip flop into J-K flip flop
iii) J-K flip flop into D flip flop
iv) J-K flip flop into T flip flop

(b) Explain the working of CMOS NAND and NOR gates. Give its specifications. **(10)**

Q5 **(a)** i)What is Hamming code? For the data bits 1011 construct even parity 7 bit Hamming code. **(10)**
ii) If Hamming code received as 1111101. What is the corrected code? Assume even parity.

(b) Explain Mealy and Moore Machines in details **(10)**

Q6 Write short note on following, **(20)**
i) Excess 3 Code
ii) De Morgan's Theorem
iii) Universal Shift Register
iv) CPLD and FPGA Architecture

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