Duration: 3hrs **[Max Marks: 80]**

N.B. : (1) Question No 1 is Compulsory.
(2) Attempt any three questions out of the remaining five.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

1 Attempt **any FOUR** **[20]**

a Explain the reverse bias mode of operation of the P-N junction diode with neat sketch.

b Explain the operation of the photo diode with neat sketch.

c Compare or differentiate between clipper & clamper circuits.

d Derive an expression for the ripple factor (γ) of a full wave bridge type rectifier.

e Explain the operation of inductor (L) type filter with neat sketch.

2 **a** Describe the working or operation of a center-tapped type full wave rectifier with a neat sketch. Draw the input voltage & output voltage waveforms. **[10]**

b For any full wave rectifier, derive the output voltage expressions for AC output voltage (V_{rms}) & DC or average (V_{dc}) output voltage. **[10]**

3 **a** With appropriate mathematical analysis, explain the effect of temperature on the P-N junction diode V-I characteristics. **[10]**

b Explain with the help of neat diagram explain the working of light emitting diode (LED). **[10]**

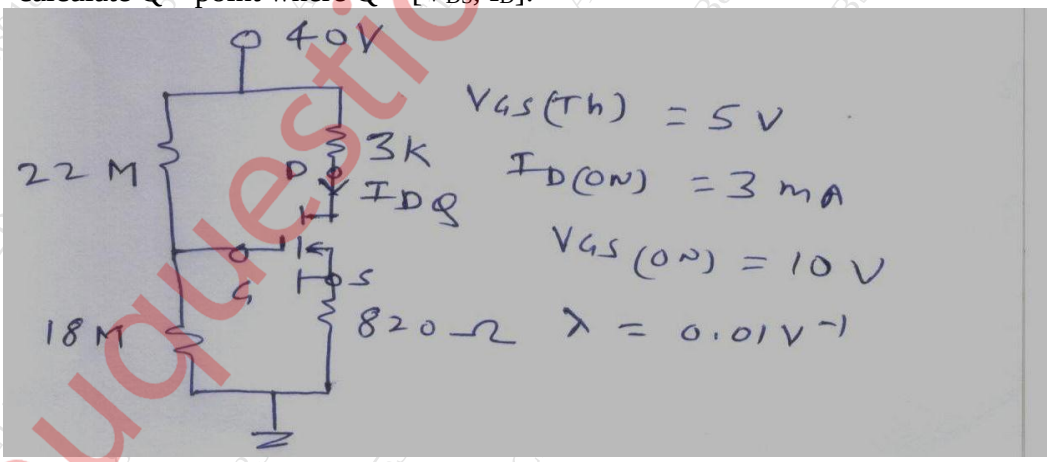
4 **a** Compare Zener breakdown & avalanche breakdown. Describe the reverse bias characteristics of Zener diode with neat sketch. **[10]**

b What are memristors ? Explain the operating principle, construction & working of memristors with a neat sketch. **[10]**

5 **a** Compare different biasing circuits of a bipolar junction transistor (BJT). **[10]**

b Draw circuit diagram and explain the operation of different biasing circuits used for D-MOSFET. **[10]**

6 **a** For the voltage divider bias circuit shown below using N-channel E-MOSFET calculate Q – point where Q = [V_{DS}, I_D]. **[10]**



b For small signal amplifier in common emitter (CE) BJT configuration using voltage divider biasing perform small signal (AC) analysis using the hybrid – π model. **[10]**

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Time: 3 Hrs **Marks: 80**

NB: (1) Question No. 1 is Compulsory.
(2) Attempt any three questions out of remaining five.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

Q.1 Answer any four

a) Convert the decimal number (123)10 to their octal, hexadecimal, BCD and gray code equivalent. 5M

b) Explain characteristics of logic families. 5M

c) Design and implement full adder circuit. 5M

d) Write a short note on Hamming code. 5M

e) Explain the working of a two –inputs CMOS NOR gate with neat diagram 5M

f) Explain the structural VHDL description of 2 to 4 decoder in detail. 5M

Q.2 a) Draw the circuit diagram of TTL NAND gate with totem pole output and explain its working with the help of a truth table. 10M

Q.2 b) Design and implement the following expression using a single 8:1multiplex**er**

F(A,B,C,D)=∑m(0,1,3,4,8,9,15). 10M

Q.3 a) Design and implement D FF using JK FF and T FF using SR FF 10M

Q.3 b) Explain the working of 3 bit asynchronous counter with proper timing diagram 10M

Q.4 a) What is shift register? Explain any one type of shift register. Give its application. 10M

Q.4 b) Reduce the following state table using partitioning method of state reduction. 10M

PS	Next State		Output	
	X=0	X=1	X=0	X=1
S0	S1	S2	0	0
S1	S3	S4	0	0
S2	S5	S6	0	0
S3	S0	S0	0	0
S4	S0	S0	1	0
S5	S0	S0	0	0
S6	S0	S0	1	0

Q.5 a) Implement following function using PLA. 10M

F1=$\sum m = (0,1,3,4)$ and F2=$\sum m = (1,2,3,4,5)$

Q.5 b) Design 2 bit comparator and implement using logic gates. 10M

Q.6 a) Implement and explain 4 bit BCD adder using IC 7483 10M

Q.6 b) Write a Verilog code for 8:1 multiplexer using data flow modelling. 10M