10/06/2025 SE CSE-AIML SEM-III C-SCHEME DLCA QP CODE: 10081925

Time :(3 hours)   **Total Marks: 80**

N.B.   1. Question **No. 1** is compulsory
         2. Attempt any **three** questions from remaining five questions
         3. Assume suitable data if **necessary** and justify the assumptions
         4. Figures to the **right** indicate full marks

Q1	A	Explain the Register organization of processor	**05**
	B	Describe the Full Adder circuit with a neat diagram and truth table	**05**
	C	Explain the IEEE 754 standards for representation of floating point numbers	**05**
	D	Draw the detailed Von-Neumann Architecture and explain in brief	**05**
Q2	A	Draw the flow chart of Non Restoring division algorithm and Perform $6 \div 2$	**10**
	B	Explain the instruction cycle with the help of a neat state diagram	**10**
Q3	A	Draw the Flowchart for the Booth's Algorithm for signed integer multiplication and perform the multiplication between 6 and 2 using this Algorithm	**10**
	B	Explain the various methods of designing a hardwired control unit	**10**
Q4	A	Consider a fully associative mapped cache with block size 4 KB. The size of main memory is 16 GB. Find the number of bits in tag.	**10**
	B	Explain Flynn's classification	**10**
Q5	A	What is the difference between Computer organization and Computer architecture explain it with a example	**05**
	B	Differentiate between Interleaved and Associative Memory	**05**
	C	Explain Instruction pipelining and the hazards associated with it .	**10**
Q6		Write short notes on	**20**
	A	.Logic Gates	
	B	Flip Flops	
	C	Cache Coherence	
	D	PCI Bus	

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