S.E. / COMP / Sem-III / 'C' Scheme / Sub:- DL & CA / Date:- 20/11/25 / 5.11.2025
QP. Code:- 10096788

Time: 3 hours **Max. Marks: 80**

Instructions:
1) **Question Number 1 is compulsory.**
2) Solve any **three questions** out of **remaining five** questions.
3) Each Question carries 20 marks.
4) Illustrate your answers with neat sketches wherever necessary.
5) Figures to the right indicate full marks.
6) Assume suitable additional data, if necessary and clearly state it.
7) All sub-questions of the same question should be grouped together.

Q.1	**(a)**	What are the advantages and disadvantages of the Von Neumann architecture?	**05**
	(b)	Represent 4.5 in IEEE 754 Single precision Format.	**05**
	(c)	Explain the difference between a MUX and a DMUX with suitable parameters.	**05**
	(d)	Write a microprogram for the instruction ADD R_3, R_4.	**05**
Q.2	**(a)**	A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words. a) How many bits are required for addressing the main memory? b) How many bits are needed to represent the TAG, SET and WORD fields?	**10**
	(b)	Explain the different methods of Centralized BUS Arbitration.	**10**
Q.3	**(a)**	Compare with suitable parameters a microprogrammed control unit and hardwired control unit.	**10**
	(b)	Explain the various addressing modes.	**10**
Q.4	**(a)**	Explain how the NAND gate can be used as a universal logic gate. Provide examples of how it can be used to implement other logic gates.	**10**
	(b)	Multiply 13 x -6 using Booth's Multiplication Algorithm.	**10**
Q.5	**(a)**	With the help of algorithm for non-restoring division perform the division operation on $(46)_{10}$ and $(23)_{10}$. Show the intermediate steps involved in the division process and explain how the final result is obtained.	**10**

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	(b)	List and describe the typical stages of a classic instruction pipeline in a CPU. What is Pipeline Hazard? Explain the types of pipeline hazards.	**10**
Q.6	**(a)**	Draw instruction cycle state diagram with interrupt.	**03**
	(b)	Give the methods used for design of Hardwired Control unit?	**03**
	(c)	What is Cache Memory? A 32-bit computer has a 32 bit memory address. It has 8kB of cache memory. The computer follows four-way set associative mapping. Each line size is 16 bytes. Show the memory address format and cache memory organization.	**05**
	(d)	List the different levels of the memory hierarchy, from the fastest to the slowest.	**04**
	(e)	Draw the block diagram for the MIMD architecture under Flynn's Classification and explain its components.	**05**

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