June 12, 2024 02:30 pm - 05:30 pm 1T01873 - S.E. Computer Science & Engineering (Artificial Intelligence & Machine Learning) (R-2019)(C-Scheme) SEMESTER - III / 49374 - Digital Logic & Computer Architecture QP CODE: 10057566

(Time: 3 hours) **(Total Marks: 80)**

N.B. 1. Question **No. 1** is compulsory
2. Attempt any **three** questions from remaining five questions
3. Assume suitable data if **necessary** and justify the assumptions
4. Figures to the **right** indicate full marks

Q1	a	Draw the Detailed Von- Neumann architecture and explain in brief	05
	b	Explain IEEE-754 Floating point Representation	05
	c	Explain the difference between Encoder and decoder	05
	d	Differentiate between Hardwired control unit and Micro programmed control unit	05
Q2	a	List out the basic and universal logic gates with the symbol, truth table, output expression	05
	b	What do you mean by BCD? Perform 792 + 128 using BCD addition	05
	c	Explain the various Addressing Modes	10
Q3	a	What is the difference between Computer organization and Computer architecture explain it with a example	05
	b	List & explain the characteristics of memory	05
	c	Draw the Flowchart for the Booth's Algorithm for signed integer multiplication and perform the multiplication between -6 and 2 using this Algorithm	10
Q4	a	List the various methods to design the Hardwired control unit and explain any one	05
	b	Explain the Micro instruction format	05
	c	Explain Flynn's Classification	10
Q5	a	List and explain the various pipeline Hazards	05
	b	Write a microprogram to represent the Interrupt cycle	05
	c	Consider a 2-way set associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find- 1. Number of bits in tag 2. Tag directory size	10
Q6	a	Represent -7.14 using double precision format of IEEE 754 standards	05
	b	Explain the concept of locality of reference	05
	C	Explain the various Bus arbitration methods	10