Paper / Subject Code: 49374 / Digital Logic & Computer Architecture 14/12/2024 CSE-AIML SEM-III C SCHEME DLCA QP CODE: 10070846 (3 hours) Total Marks: 80

	N.B.	1. Question No. 1 is compulsory	
		2. Attempt any three questions from remaining five questions	
		3. Assume suitable data if necessary and justify the assumptions	
		4. Figures to the right indicate full marks	
Q1	A	What are universal logic gates? Why are they called so? Explain with a suitable	05
	_	example	937
	В	Explain the functioning of D and T flip-flops along with their Truth table	05
	C D	Differentiate between Hardwired control unit and Micro programmed control unit List and describe the key characteristics of memory?	05 05
Q2	A	Using booths algorithm multiply 3 x -2 along with its flow chart do write appropriate	10
		comments for each operation.	
	В	Draw the flow chart for Restoring division algorithm and Perform 6 ÷3	10
0.2	15		1.0
Q3	A	Explain Multiplexer & Demultiplexerx (IC level description only)	10
	В	Discuss the different ways in which data can be accessed in memory using addressing modes.	10
Q4	A	Explain Micro instruction format and write a micro program for the instruction	10
		$ADD R_1, R_2$	
	В	Explain Hardwired Control Unit and the various design methods associated with it.	10
Q5	A	Explain different memory Mapping Techniques	10
7	В	Describe Interleaved memory	05
	C	What do you mean by cache coherence	05
Q6	A	Explain Instruction pipelining and describe the hazards associated with it	10
	В	Explain Flynn's Classification.	10
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