Paper / Subject Code: 49374 / Digital Logic & Computer Architecture

1T01873 - S.E. Computer Science & Engineering (Artificial Intelligence & Machine Learning) (R-2019) SEMESTER - III / 49374 - Digital Logic & Computer Architecture

QP CODE: 10014070   DATE:29/11/2022   (3 hours)   Total Marks: 80

N.B.   1. Question **No. 1** is compulsory
       2. Attempt any **three** questions from remaining five questions
       3. Assume suitable data if **necessary** and justify the assumptions
       4. Figures to the **right** indicate full marks

Q1   A   Convert   05
         i) 123 in to binary
         ii) $(AB9)_{16}$ in to Decimal
         iii) $(351)_8$ in to decimal
         iv) 129 in to BCD
         v) 64 in to gray code

    B   Draw the single and double precision format for representing floating point number   05
Q1   using IEEE 754 standards and explain the various fields
    C   Explain SR Flip Flop   05
    D   Differentiate between Hardwired control unit and Micro programmed control unit   05

Q2   A   Draw the flow chart of Booths algorithm for signed multiplication and Perform -   10
       5 x 2 using booths algorithm

    B   Explain the different addressing modes.   10

Q3   A   For 132.65 obtain the IEEE 754 standards of Single precision and Double precision   10
       format
    B   Explain Micro instruction format and write a microprogram for the instruction   10
       ADD R_1 , R_2

Q4   A   Consider a 4-way set associative mapped cache with block size 4 KB. The size of the   10
       main memory is 16 GB and there are 10 bits in the tag. Find-
       1. Size of cache memory
       2. Tag directory size

    B   Explain Flynn's classification   10

Q5   A   Explain different types Distributed and Centralized bus arbitration methods   10

    B   Describe the detailed Von-Neumann Model with a neat block diagram   05

    C   Describe the characteristics of Memory.   05

Q6   Write Short notes on   20

       a) Grey code, BCD, Excess-3 Code with example

       b) Encoder and Decoder

       c) Cache coherence

       d) Instruction Pipelining

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