S.E. (Instrumentation) Sem. III choice based Dt 24/5/19 (1/1)

(3 Hours) [Total Marks: 80]

N.B: (1) **Question No. 1** is **compulsory**.
(2) Attempt any **THREE** questions from remaining.
(3) **Figures** to the **right** indicate **full marks**.
(4) Assume suitable **data** if **necessary**.

1. Answer the following: - [20]
   (a) Convert $(123.091)_{10}$ to Octal and Binary.
   (b) Verify De Morgan's Theorem.
   (c) Convert JK flipflop to T flipflop.
   (d) Design Half Adder circuit.

2. (a) Simplify using K-Map [10]
   i) $Y = \sum m\,(4,5,7,12,14,15) + d\,(3,8,10)$
   ii) $Y = \sum m\,(0,1,2,3,5,7,8,9,11,14)$
   (b) Perform: - i) $(29)_{10} - (33)_{10}$ using 2's complement method. [10]
   ii) $(123)_{16} * (ABC)_{16}$

3. (a) Design 4 bit Binary to Gray code converter. [10]
   (b) Design two-bit magnitude Comparator using logic gates. [10]

4. (a) Design Mod 5 synchronous counter using JK flip- flop. [10]
   (b) Explain with a neat diagram working of SISO shift register. Draw necessary timing diagram. [10]

5. (a) Explain working of static and dynamic RAM cell. [10]
   (b) Design and implement a full subtractor circuit using 3: 8 Decoder. [10]

6. Write note on: - **(Any Four)** [20]
   (a) FPGA.
   (b) Hazards and Hazard elimination.
   (c) Johnson Counter.
   (d) ECL Family.
   (e) Priority Encoder

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