

Time: 3 Hours

Marks: 80

- N.B. : (1) Question No. 1 is compulsory.
 (2) Solve any three questions from the remaining five
 (3) Figures to the right indicate full marks
 (4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt any 5 questions **[20]**

- a) Prove that for a JFET the gate-source bias for zero temperature drift of drain current is at $|V_p| - 0.63$ volts.
- b) Explain the hybrid pi model of BJT.
- c) Explain Zener as voltage regulator.
- d) Consider a BJT has parameters $f_T = 500\text{MHz}$ at $I_C = 1\text{mA}$, $\beta = 100$ and $C_{\mu} = 0.3\text{pF}$. Calculate bandwidth of f_{β} and capacitance C_{π} of a BJT.
- e) Draw and explain small signal model of a diode.
- f) Why should R_C be as large as possible in the design of CE amplifier?

Q.2 a) Design a voltage divider bias network using a supply of 24 V, a transistor with $\beta=110$ and an operating point of $I_{CQ} = 4 \text{ mA}$ and $V_{CEQ} = 8\text{V}$. Assume **[10]**

$$V_E = \frac{1}{8} V_{CC}$$

- b) Explain the fabrication steps of passive elements. **[5]**
- c) What are the important JFET parameters and define it from characteristics. **[5]**

Q.3 a) Design the resistors of a single stage CS amplifier for audio frequency with BFW11 with $I_{DS} = (3.3 \pm 0.6) \text{ mA}$ and $|A_v| = 12$. **[10]**

- b) Draw CS JFET amplifier with self bias circuit and derive the expression for voltage gain input impedance and output impedance. **[10]**

Q.4 a) Draw small signal hybrid parameter equivalent circuit for CE amplifier and define the same. What are the advantages of h parameters? **[10]**

- b) For the circuit shown below in Fig.4b, the transistor parameters are $V_{BE(\text{on})} = 0.7 \text{ V}$, $\beta = 200$ and $V_A = \infty$. **[10]**
 - i) Derive the expression for lower cut-off frequency (or time constant) due to input coupling capacitor.
 - ii) Determine lower cut-off frequency and midband voltage gain.

TURN OVER

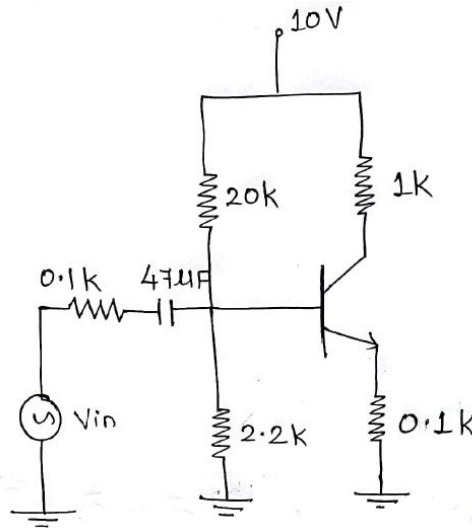


Fig.4b

Q.5 a) Design an L section LC filter with full wave rectifier to meet the following [10]
 specifications: The DC output voltage $V_{dc} = 220$ V, deliver $I_L = (70 \pm 20)$ mA to the resistive load and the required ripple factor is 0.04.

b) For the circuit shown below in Fig.5b, the transistor parameters are $V_{BE(on)} = 0.7$ V, $\beta = 100$ and $V_A = \infty$. Determine Z_i , Z_o and A_v [10]

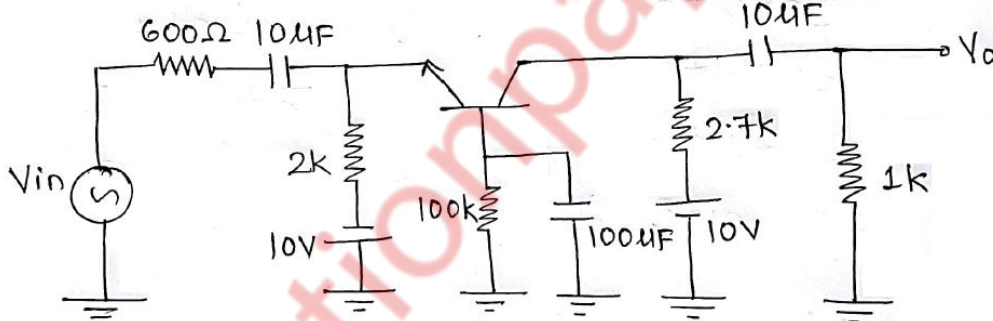


Fig. 5b

Q.6 Short notes on: (Attempt any four) [20]

- BJT high frequency equivalent circuit
- Types of resistors and capacitors
- Stability factors of various biasing techniques of BJT
- Different types of filters
- Comparison of BJT CE and JFET CS amplifier

TURN OVER

Transistor type	F _{max} (MHz) @ 25°C	V _{CE} (V) d.c.	V _{CE} (V) d.c.	V _{CE} (V) d.c.	V _{CE} (V) d.c.	V _{CE} (V) d.c.	V _{CE} (V) d.c.	V _{CE} (V) d.c.	V _{CE} (V) d.c.	D.C. current		Small signal	f _h max.	V _{CE} max.	Derate above 25°C
										Watts	Amperes				
2N 3055	115-5	15-0	1-1	100	60	70	90	7	200	20	50	15	50	1-8	0-7
EGN 055	50-0	5-0	1-0	60	50	55	60	5	200	25	50	25	75	1-5	0-4
EGN 149	30-0	4-0	1-0	50	40	—	—	8	150	30	50	33	60	1-2	0-3
EGN 100	5-0	0-7	0-6	70	60	65	—	6	200	50	90	280	200	0-9	0-03
BC147A	0-25	0-1	0-25	50	45	50	—	6	125	115	180	125	270	280	—
2N 525(PNP)	0-225	0-5	0-25	85	30	—	—	—	100	35	—	65	45	—	—
BC147B	0-25	0-1	0-25	50	45	50	—	6	125	200	290	450	330	500	—

BFW 11—JFET MUTUAL CHARACTERISTICS

-V _{GS} volts	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}	I _{DS}
0-0	0-2	0-4	0-6	0-8	1-0	1-2	1-6	2-0	2-4	2-5	3-0	3-5	4-0	—	—
1-0	9-0	8-3	7-5	6-8	6-1	5-4	4-7	3-1	2-2	2-0	1-1	0-5	0-0	—	—
2-0	6-0	5-4	4-6	4-0	3-3	2-7	1-7	0-8	0-2	0-0	0-0	0-0	0-0	—	—
3-0	3-0	2-2	1-6	1-0	0-5	0-0	0-0	0-0	0-0	0-0	0-0	0-0	0-0	—	—

M-Channel JFET

Type	V _{GS} max. Volts	V _{GS} max. Volts	V _{GS} max. Volts	P _d max. @25°C	I _{DS} max.	I _{DS} (typical)	-V _{GS} Volts	f _s	Derate above 25°C
2N5822	50	50	50	300 mW	175°C	2 mA	3000 μC	50 KΩ	0-50°C/mW
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μC	50 KΩ	0-50°C/mW

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