S.E. EXTE Sem III (CBQJ).

3/12/15

Digital Electronics

QP Code : 5174

		(3 Hours) To	tal Marks: 80
		(3 Hours) To Question No. 1 is Compulsory Out of remaining questions, attempt any three Assume suitable data if required Figures to the right indicate full marks Compare SRAM and DRAM Compare Mealy and Moore machine Compare TTL and CMOS Logic Design a full adder using 3:8 decoder State and Prove DeMorgan's Laws Explain carry look ahead adder. What is its advantage over a simple of the state over a state over a simple of the state over a state over a simple of the state over a	0°
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11110	(1) (2)	Question No. 1 is Compulsory	
	(2)	Out of remaining questions, attempt any three	Š.
	(4)	Assume suitable data if required	
	(4)	Figures to the right indicate full marks	2
1.	(a)	Compare SRAM and DRAM	151
	(b)	Compare Mealy and Moore machine	()
	(c)	Compare TTL and CMOS Logic	[5]
	(d)	Design a full adder using 3:8 decoder	[5] (6)
			(5)
2.	(a)	State and Prove DeMorgan's Laws	1101
	(b)	Explain carry look ahead adder. What is its advantage over a simple add	[10] ler [10]
3.	(a)		[~~]
	(•)	Design a 4 bit Grey to Binary code converter	[10]
	()		[10]
	10.2	$F(A, B, C, D) = \sum m(0,1,4,5,6,8,10,12,13)$	
4.	(a)	Explain the working of Bidiroctional Stie	
	(b)	Explain the working of Bidirectional Shift register with proper timing di Write a VHDL program to design a 1:8 Demux using Data flow modelin	agram [10]
	``	program to design a 1.8 Demux using Data flow modelin	ig [10]
	(a)	Minimize the following expression using Quine McClusky Technique	1
	``	$F(A,B,C,D) = \sum m(1,2,5,7,9,15) + d(0,3,11)$	[10]
	(b)	Convert D FF to TFF and SR FF to JK FF	
			[10]
6.	(a)	Design synchronous counter to count the sequence 0-1-2-3-4-5-0	14.0-
I			[10]
			[10]
		Compare PAL with PLA with suitable examples of logic expressions	
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