Q. P. Code : 40468

[Time: 3 hours] [Max Marks 80]

1) Question no. 1 is compulsory
2) Solve any three from the remaining five questions.
3) Assume suitable additional data if necessary.

Q1) Answer the following questions: (20)
a) Explain the feature of pipelining and queue in 8086 architecture.
b) Explain the significance of TEST*, RESET and MN/MX* signals in 8086 processor
(* indicates bar).
c) List the steps taken by 8086 processor in response to receiving an interrupt.
d) In 8086 bus cycle, explain the significance of ALE signal.
e) Explain the flag register for 8086 processor.

Q2)a) List and explain with examples addressing modes of 8086 processor. (10)
b) Explain with the help of neat diagram interfacing of 8086-8087 closely coupled configuration system. (10)

Q3)a) With the help of memory map interface the following to an 8086 based system operating in minimum mode: (14)
a) 32K bytes of EPROM memory using 8k byte devices.
b) 32K bytes of RAM memory using 8k byte devices.
c) One 16 - bit input and output port.
b) Explain the following 8086 instructions (ANY THREE)
a) CMPSB b) DIV AX c) LOOPE again d) REP SCASB e) XLATB (06)

Q4) a) Write a detailed note on the interrupt structure of 8086 processor. (10)
b) Explain the need for DMA and modes of DMA data transfer typically made use of by the DMA controller IC - 8237. (10)

Q5) a) b) Explain the Intel Pentium processor's pipelining and superscalar architecture. (10)
b) With the help of a neat flowchart/algorithm write a program in 8086 assembly to arrange a set of ten 8-bit numbers initialized in data segment in ascending order. (10)

Q6) Write short notes on: [ANY TWO]
a) Programmable interrupt controller – 8259. (10)
b) Intel Pentium processor – Branch Prediction Logic (10)
c) Programmable peripheral interface – 8255, need for and operation in Mode – 1. (10)

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