Q.P. Code:00906

[Time: 2 Hours]

[Marks:75]

(15)

54-21 10-49 82 20 100 8421

Please check whether you have got the right question paper.

- N.B:
- 1. All questions are compulsory.
- Make suitable assumptions wherever necessary and state the assumptions made.
- Answer to the same question must be written together.
- Numbers to the right indicate marks.
- Draw neat labeled diagrams wherever necessary.
- 6. Use of Non-programmable calculators is allowed.

Attemptany three of the following:

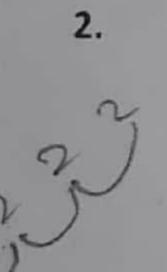
- Write the difference between analog signal and digital signal.
- Convert the following numbers b. $(17E.F6)_{16} = (?)_2$ $(110010100011.10100101)_2 = (?)_2$
- Convert the given $(125.50)_{10} = (?)_2$ $(110001)_2 = (?)_{10}$
- Find
 - i) The Gray code equivalent of Decimal (13)
 - ii) Binary equivalent of Gray code 1111.
 - iii) Hexadecimal equivalent of octal (765)
 - iv) Octal equivalent of binary(1100111110101)
 - v) Decimal equivalent of binary 1010101010.
- Write a short note on Error correction and detection code.
- i) Perform the addition of following Binary number (1100010 + 1010001)
 - ii) Perform the Subtraction of following Binary numbers using 1's complement method. (11011 - 10001).

Attemptany three of the following:

- For the logic expression Y=AB+A'B' Obtain the truth table, name the operation performed, realize the operation using AND, OR, NOT gate. Also realize it using NAND gate only.
- Draw the output wave form of AND gate and explain it's operation. Also, discuss about 4 input AND gate.
- Prove the following using Boolean law A+A'. B + A.B' = A+B
- Reduce the given SOP equation using K-map method and draw the circuit using NAND network. ABC + ABC'+AB'C' + A'BC.
- Reduce the given POS function using K-map and draw the circuit diagram using NOR network F(A,B,C,D) = [(0,1,2,3,7,8,9,10,11)]
- Using Don't care condition find reduced SOP equation and draw the circuit diagram using basic gates

 $F(P,Q,R,S) = \sum (1,2,3,6,12,14) + d(0,11,13)$

[TURN OVER]



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3. Attemptany three of the following:

Design the Half adder using K-map. Draw the circuit diagram for the same.

- b. With the help of circuit diagram discuss four bit binary adder-subtractor.
- c. Design two bit magnitude comparator.
- d. Write a short note on BCD to EXCESS-3 code converter.
- e. What is Multiplier? Draw diagram and explain 4x4 bit multiplier.
- f. Explain Full Adder in detail.

4. Attemptany three of the following:

- a. Draw the logic diagram of 4 to 1 multipexer. Explain its working.
- b. Write a short note on demultipexer.
- c. Define cascading. Design 16 to 1 multipexer using 8 to 1 multipexer.
- d. With the help of diagram explain Bistable Multivibrator.
- e. What is meant by race around problem? Explain master slave flip-flop.
- f. How J-K flip-flop can used to form a D flip-flop.

Attemptany three of the following:

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- a. Write a short note on modulus of counter.
- b. Explain the working of four bit UP/DOWN counter.
- c. Determine the number of flip-flops in Mod 10 ring counter and Jonson counter. Write count sequence in both the cases.
- d. Briefly describe the architecture of SISO shift register.
- e. Explain the design procedure for MOD 8 binary counter.
- f. The table gives below the excitation of flip-flop having inputs X1 and X2. Draw the circuit excitation table of Mod -5 synchronous conter using this flip-flop for the counter sequence 000,001,010,011,100,000. Design the counter using flip-flop whose excitation table is given below.

Preset state (Qn)	Next state (Qn+1)	Input (X1)	Input (X2)
0	0	0	0
0		0	1
1	0	1	X
1	1	X	

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