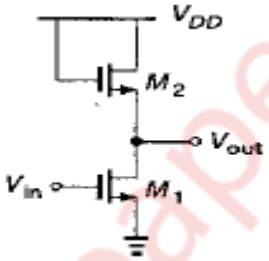
Time: 3 Hours **Max Marks: 80**

N.B. 1) Question No.1 is compulsory
2) Solve any three questions from the remaining questions.
3) Assume suitable data if necessary.

1 Solve any four of the following.

(a) Explain trade-offs in analog design with the help of analog design octagon 5
(b) For a n-channel MOSFET draw- a)a basic small signal model b) small signal model considering channel length modulation effect c) small signal model considering body effect 5
(c) Explain the concept of clock feed through in the MOSFET sampling circuit 5
(d) Compare performance of various op-amp topologies 5
(e) Derive expression for input referred noise of CS stage 5

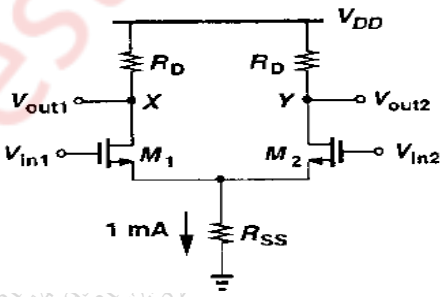
2 (a) 10



Identify the above network .Derive the gain equation of the above circuit.

(b) Derive equation of differential gain, common mode gain and CMRR of a differential amplifier circuit. 10

3 (a) The following circuit uses a resistor rather than a current source to define a tail 10

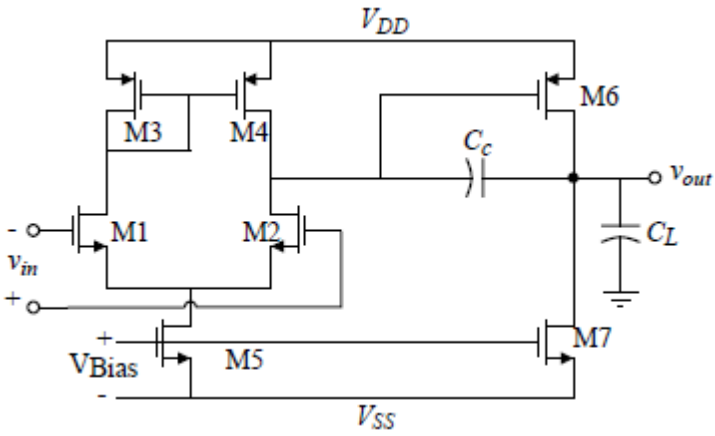


current of 1mA.

Assume $(W/L)_{1,2}=25/0.5$, $\mu_n C_{ox}=50\mu A/V^2$, $V_{TH}=0.6V$, $\lambda=0$, $V_{DD}=3V$
(a)What is the required input CM for which Rss sustains 0.5V?
(b)Calculate R_D for a differential gain of 5
(c) What happens at the output if input CM level is 50mV higher than the value calculated in (a)?

(b) Derive expression for voltage gain A_V and output resistance Ro of source follower stage. 10

Q.4 Design two stage operational amplifiers that meet the following specifications 20



Av > 3000V/V V_{DD} =2.5V V_{SS}=-2.5V
Gain Bandwidth = 5MHz, Slew Rate > 10V/µs, 60° phase margin,
0.5V< V_{out} range <2V,
ICMR = -1.25V to 2V,
$P_{diss} \leq 2$ mW, C_L=10pF
Use $K_N' = 100\mu A/V^2$, $K_P' = 20\mu A/V^2$, $V_{TN} = |V_{TP}| = 0.5V$, $\lambda_N = 0.06V^{-1}$,
$\lambda_P = 0.08V^{-1}$, Cox=2.47fF/µm^2.
Verify that the designed circuit meets required voltage gain and power dissipation specifications

5 (a) Explain the charge injection mechanism in MOS sampling circuits and also describe the errors contributed by the above effect. 10

(b) What is a band gap reference? Describe methods of implementation of band gap references 10

6 Write short note on any four

(a) Necessity of Millers theorem 5

(b) Gilbert Cell 5

(c) Charge Pump PLL 5

(d) Comparison of full custom design and semi custom design 5

(e) Performance parameters of VCO 5

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