## Paper / Subject Code: 53001 / CMOS VLSI Design

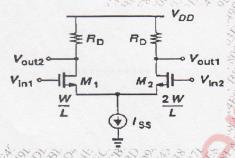
Sem-VIII - ETRX - CBSGS - NOVIDER. 20.11.18

Time: 3 Hours

Max Marks: 80

5

- N.B. 1) Question No.1 is compulsory
  - 2) Solve any three questions from the remaining questions.
  - 3) Assume suitable data if necessary.
  - 1 Solve the following.
    - (a) Analyze following circuit to get voltage gain equation if M2 is twice wide as that of M1 and Vin1=Vin2



- (b) Explain the concept of switched capacitor circuit
- (c) Compare performance of various op-amp topologies 5
- (d) Explain System on Chip and System in Package.
- 20 (a) Design two stage operational amplifiers that meet the following specifications 20 with a phase margin of 60. Assume the channel length is to be 1 $\mu$ m, KN'=100 $\mu$ A/V2, KP'=20 $\mu$ A/V2, VTN = |VTP| = 0.5V,  $\lambda_N$  = 0.06V-1, and  $\lambda_P$  = 0.08V-1 Av>5000v/v, Vdd=2.5V, Vss= -2.5v ,GBW=5MHz , C<sub>L</sub>=10pf , SR>10v/ $\mu$ sec, Vout range=+/- 2V, ICMR=-1 to 2V, P<sub>diss</sub> $\leq$  2mw..
- (a) Derive expression for voltage gain AV and output resistance Ro of source 10 follower stage.
  - (b) Compare full custom and semi-custom design in terms of its trade-off and 5 applications.
  - (c) Explain Non-ideal effects in PLL. 5
- 4 (a) Derive equation of differential gain, common mode gain and CMRR of 10 differential amplifier.
  - (b) Explain White & Flicker noise in MOSFET. Derive equation for output and 10 input referred noise voltage of CS stage
- 5 (a) Draw and explain AMS design flow.
  - (b) Draw and explain discrete time integrator along with the output waveform.

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