B.E Sem VII CBGIS <u>Electronics</u>. 23-11-2015 Embedded System Denign QP Code: 5860

(3 Hours)

ITotal Marks: 80

(20)

PJ.6

- 1) Question no. 1 is compulsory
- 2) Solve any three from the remaining five questions.
- 3) Assume suitable additional data if necessary.
- Answer the following questions. Q1
 - a) With the help of an example explain periodic task. List and explain the various types of tasks in an embedded system.
 - b) With respect to power, performance and cost state and explain the associated design metrics for an embedded system.
 - c) What are interrupts and explain the factors that contribute to interrupt response time in a system.
 - d) Explain the structure of typical C source program for ARM based target processor. Typically list the various data types along-with memory size supported by a C compiler.

Q2 a) What is a task and various states that a task can lie in for an embedded (10)environment.

b) Explain briefly the problem of priority inversion and mechanism to prevent (10)the same.

Q3) a) State and explain the criteria for tasks schedulability and explain various (10)scheduling mechanisms.

b) Explain briefly the register structure of Cortex-M3 architecture along-with (10) the function of various special registers.

Q4) a)Distinguish between Cortex – M3 and M4 architecture and explain briefly the interrupt structure of M3 architecture. (08)

Explain the operation and significance of following MicroC/OS - II b) (12)functions.(Any Three)

a) OSInit(); b) OSSemPend(); & OSSemPost(); c) OSTaskCreate();

d) OSMboxPost(); & OSMboxPend();

Q5) a) Write a brief note to bring out the comparision between Cortex -M3, A8 (10)and R4 architectures.

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(20)

b) Explain the various inter- process/task communication tools like pipe, mailbox, message queue and semaphore used by an RTOS environment. (10)

Q6) Write short notes on (Any two)

- a) Serial communication standard RS-232 and comparison with RS 485.
- b) Low power features in Cortex M 3 architecture.

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c) Black box and White box testing.

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