Q. P. Code: 35474

(3 Hours) Total Marks: 80

N.B. (1) Question No. 1 is Compulsory
(2) Out of remaining questions, attempt any three
(3) Assume suitable data if required
(4) Figures to the right indicate full marks

Q.1 (a) State and prove De Morgan’s Theorems [5]
(b) Compare Combinational and sequential logic Circuits [5]
(c) Define Propagation delay, Power Dissipation, Fan Out, Fan in for TTL family [5]
(d) Explain Programmable Logic Array [5]

Q.2 (a) Prove that NAND and NOR Gates are universal Gates [10]
(b) Design a two-bit digital comparator and implement using Gates [10]

Q.3 (a) Simplify the logical expressions using Boolean Laws and implement using Gates [10]
\[ Y_1 = (A + C)(A + D)(B + C)(B + D), \quad Y_2 = (AB + C)(AB + D) \]
(b) Implement the given function using 8:1 Multiplexer [10]
\[ F(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 6, 8, 9, 10, 12, 13, 15) \]

Q.4 (a) Explain the working of universal shift register [10]
(b) Write a VHDL program to design a 4:1 Mux [10]

Q.5 (a) Minimize the following expression using Quine McClusky Technique [10]
\[ F(A, B, C, D) = \sum m(1, 3, 7, 9, 10, 11, 13, 15) \]
(b) Convert JK FF to D FF and T FF to D FF [10]

Q.6 (a) Design a 3-bit asynchronous counter using JK FF. Draw neat timing diagram [10]
(b) Write a note on CPLDs [10]

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