(3 Hours)  [Total Marks : 80]

N.B. (1) Question no 1 is compulsory
(2) Out of remaining questions, attempt any three questions
(3) Assume suitable data if required
(4) Figures to the right indicate full marks

1. (a) Compare combinational logic circuits with sequential circuits
      (b) Compare PLA and PAL
      (c) Explain static RAM
      (d) Explain Master-Slave JK Flipflop

2. (a) State and prove laws of Boolean Algebra
      (b) Using Quine McClusky method, minimize the following
          \[ F(A, B, C, D) = \sum m(0, 2, 5, 7, 8, 10, 12, 15) \]

3. (a) Implement Full adder using 8:1 multiplexers
      (b) Write VHDL code for 3-bit up counter

4. (a) Design a two bit digital comparator and implement using basic logic gates
      (b) Draw a neat circuit of BCD adder using IC 7483

5. (a) What is universal shift register? Explain any two modes of shift register
      (b) i) Covert a D FF to T FF
          ii) Convert a JK FF to T FF

6. (a) Design a synchronous counter using 1 FF for the sequence given below:
      \[ 1-2-3-4-5-6-7-1 \]
      (b) Define the following terms for logic families
          i) Propagation Delay
          ii) Fan out
          iii) Power Dissipation
          iv) Noise Margin
          v) Fan in

---