N.B. (1) Question No. 1 is compulsory.
(2) Out of remaining questions, attempt any three questions.
(3) Assume suitable additional data if required.
(4) Figures in brackets on the right hand side indicate full marks.

1. Explain the following:—
   (a) For ECL and CMOS logic families define—
       (i) noise margin (ii) fan-in (iii) fan-out.
   (b) Compare Asynchronous and synchronous counter
   (c) Explain static RAM
   (d) Explain Master-Salve J.K Flip-flop.

2. (a) Perform following operation using 2's complement method—
        (i) (28)_{10} - (42)_{10} (ii) (52)_{10} - (-18)_{10}
   (b) Prove the following using Boolean algebra.
       \[ \overline{A}BC + A\overline{B}C + ABC + AB\overline{C} = AB + BC + CA \]
   (c) Design 2 bit comparator.

3. (a) Minimum the following using Quine Mc Clusky method.
       \[ F(A, B, C, D) = \Sigma m(3, 4, 9, 13, 14, 15) + \Sigma d(5, 6) \]
   (b) Design synchronous counter using J.K flip-flop for the given sequence —
       0 - 2 - 3 - 5 - 7 - 0.

4. (a) Design following Boolean equation using 4 : 1 multiplexer
       \[ F((A, B, C, D) = \Sigma m(2, 4, 5, 7, 9, 11, 12) \]
   (b) Compare EPROM and FLASH memories.
   (c) Explain bidirectional 4 bit universal shift register.

5. (a) Explain 3 : 8 decoder.
   (b) Explain Mealy machine and Moore machine.
   (c) Write VHDL code for 3 bit binary down counter.

6. (a) Explain Architecture and features of FPGA.
   (b) Implement Fx-OR gate using NAND
   (c) Convert (118)_{10} in to (i) BCD (ii) Hexadecimal (iii) octal.

Con. 11692-14.