N.B. (1) Question No. 1 is Compulsory
(2) Out of remaining questions, attempt any three
(3) Assume suitable data if required
(4) Figures to the right indicate full marks

1. (a) Compare SRAM and DRAM
(b) Compare Mealy and Moore machine
(c) Compare TTL and CMOS Logic 
(d) Design a full adder using 3:8 decoder

2. (a) State and Prove DeMorgan’s Laws
(b) Explain carry look ahead adder. What is its advantage over a simple adder

3. (a) Design a 4 bit Grey to Binary code converter
(b) Implement the given function using 8:1 Multiplexer
\[ F(A, B, C, D) = \Sigma m(0,1,4,5,6,8,10,12,13) \]

4. (a) Explain the working of Bidirectional Shift register with proper timing diagram
(b) Write a VHDL program to design a 1:8 Demux using Data flow modeling

5. (a) Minimize the following expression using Quine McClusky Technique
\[ F(A,B,C,D) = \Sigma m(2,5,7,9,15) + d(0,3,11) \]
(b) Convert D FF to T FF and SR FF to JK FF

6. (a) Design synchronous counter to count the sequence 0-1-2-3-4-5-0
(b) Compare PAL with PLA with suitable examples of logic expressions

Total Marks: 80

MD-Con. 9620-15.