N.B.: (1) Question No. 1 is compulsory.

(2) Solve any three questions from the remaining five

(3) Figures to the right indicate full marks

(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 a) Perform the following operation using 2’s compliment
   i) \((14)_{10} - (24)_{10}\)
   ii) \((24)_{10} - (14)_{10}\)
   Comment on results of (i) and (ii)

b) If \(F(A, B, C) = \sum m(0,3,5,7)\) with its truth table and express F in SOP and POS form

c) Compare FPGA and CPLD.

d) Explain Static RAM

Q.2 a) Write VHDL code for 3 bit up counter.

b) Minimize the following expression using Quine McClusky Technique
   \(F(A, B, C, D) = \sum \{1,3,7,9,10,11,13,15\}\)

Q.3 a) Design 3 bit Binary to Gray code Converter

b) Draw and explain neat circuit diagram of BCD adder

Q.4 a) Draw and explain two input TTL NAND gate.

b) Compare combinational circuits and sequential circuits

c) Explain Full Adder circuit using PLA having three inputs, 8 product terms and two outputs.

Q.5 a) What is excitation table? Explain the excitation table of SR flip flop.

b) Convert D flip flop to T flip flop.

c) Draw and explain 3 bit asynchronous binary counter using positive edge triggered JK flip flop. Draw the waveforms.

Q.6 a) Implement following Boolean function using 8:1 multiplexer
   \(F(A, B, C, D) = \overline{ABD} + ACD + \overline{BCD} + \overline{ACD}\)

b) State and prove Demorgan’s theorem

c) What are shift registers? How are they classified? Explain working of any one type of shift register.

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