N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three from remaining five questions.
(3) Draw neat logic diagram and assume suitable data wherever necessary.

Q 1 (a) Interfacing between CMOS and TTL
(b) Explain Shift Register and its applications
(c) PLA and PAL
(d) Draw truth table and logic diagram of Full Subtractor

Q 2 (a) Write a VHDL code for Full Adder
(b) Design MOD 8 asynchronous counter.

Q 3 (a) Design a mealy sequence detector to detect 0101 using D flip-flops and logic gates
(b) Design a circuit with optimum utilization of PLA to implement the following functions

\[ F_1 = \sum_{m} (0, 2, 5, 8, 9, 11) \]
\[ F_2 = \sum_{m} (1, 3, 8, 10, 13, 15) \]
\[ F_3 = \sum_{m} (0, 1, 5, 7, 9, 12, 14) \]

Q 4 (a) Implement following function using 8:1 MUX and logic gates

\[ P(A,B,C,D) = \sum_{m} (1,2,6,7,8,10,13,14) \]
(b) Construct ring counter using IC 74194 and the output waveform

Q 5 (a) Use K-map to reduce following function and then implement it by NOR gates.

\[ F = \sum_{m} (1, 2, 5, 6, 10, 12, 15) + d (0, 5) \]
(b) Design 6 bit up counter using IC 74163. Draw a circuit diagram and explain its working.

6. Write short notes on any three
i) JTAG and BIST
ii) Stuck at '0' and '1' faults
iii) XC 4000 FPGA architecture block diagram
iv) Noise Margin

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