N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three from remaining 5 questions.
(3) Draw neat diagrams wherever necessary.

1. (A) Implement the following function using NOR gates only (after reduction using K map)
   \[ F = \pi M (1, 2, 4, 7, 11, 13) . \pi (9, 15) \]
   10
   (B) Design a MOD 6 asynchronous counter and explain glitch problem. 10

2. (A) Analyze the clocked synchronous machine given below. Write excitation equations, excitation/transition table and state/output table (Use state names A - D for Q1-Q2=00-11). Also draw the state diagram.

   \[ \text{Diagram} \]
   10
   (B) Design a 1 digit BCD adder using IC 7483 and explain the operation for \((0111)_{\text{BCD}} + (1001)_{\text{BCD}}\). 10

3. (A) Write a VHDL code for 8:1 Multiplexer with active low enable input. 10
   (B) Design a mealy sequence detector to detect a sequence 1101 using D flip-flops and logic gates. 10

4. (A) Design a circuit with optimum utilization of PLA to implement the following functions
   \[ F_1 = \Sigma m (1, 2, 3, 6, 9, 11) \]
   \[ F_2 = \Sigma m (0, 1, 6, 8, 3) \]
   \[ F_3 = \Sigma m (2, 3, 8, 9, 11) \]
   10
   (B) Implement following function using 4:1 line MUX and NAND gates.
   \[ F (A, B, C, D) = \Sigma m (1, 2, 6, 7, 8, 12, 13) \]
   10

5. (A) Design a 8 bit binary up counter using MSI counter IC 74163, draw a circuit diagram and explain working.
   (B) Eliminate redundant states and draw reduced state diagram. 10

\[
\begin{array}{|c|c|c|}
\hline
\text{PS} & \text{NS} & \text{O/P} \\
\hline
\text{A} & \text{B} & \text{C} & \text{1} \\
\text{B} & \text{D} & \text{F} & \text{1} \\
\text{C} & \text{F} & \text{E} & \text{0} \\
\text{D} & \text{B} & \text{G} & \text{1} \\
\text{E} & \text{F} & \text{C} & \text{0} \\
\text{F} & \text{E} & \text{D} & \text{0} \\
\text{G} & \text{F} & \text{G} & \text{0} \\
\hline
\end{array}
\]

6. Write short notes on (Any THREE):
   1. XC 4000 FPGA Architecture
   2. Stuck at '0' and stuck at '1' fault
   3. Master Slave JK flip flop
   4. 2 input TTL NAND gate

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