QP Code: 14602

[Total Marks: 80]

N.B.: (1) Question No. 1 is Compulsory.

(2) Solve any Three from remaining Five questions.

(3) Draw neat logic diagram and assume suitable data wherever necessary.

Q 1 (a) Interfacing between CMOS and TTL

(b) Convert T flip-flop to D flip-flop

(c) XC 4000 FPGA architecture block diagram

(d) Draw truth table and logic diagram of Full subtractor

Q 2 (a) Write a VHDL code for Full adder

(b) Design MOD 10 asynchronous counter.

Q 3 (a) Design a mealy sequence detector to detect 1010 using D flip-flops and logic gates

(b) Design a circuit with optimum utilization of PLA to implement the following functions

\[ R = \sum m (0, 2, 5, 7, 11, 12) \]
\[ P = \sum m (1, 3, 8, 9, 11, 13) \]
\[ Q = \sum m (0, 5, 8, 12, 14) \]

Q 4 (a) Implement following function using 8:1 MUX and logic gates

\[ P(X,Y,Z,W) = \sum m (0, 3, 4, 7, 8, 9, 13, 14) \]

(b) Eliminate redundant states and draw reduced state diagram

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<tr>
<th>PS</th>
<th>NS</th>
<th>O/P</th>
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<tbody>
<tr>
<td></td>
<td>X=0</td>
<td>X=\bar{0}</td>
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<tr>
<td>A</td>
<td>B</td>
<td>C</td>
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Q 5 (a) Use K-map to reduce following function and then implement it by NOR gates.

\[ F = \pi M (0, 3, 4, 5, 8, 10, 12, 14) + \pi (2, 9) \]

(b) Design 8 bit up counter using IC 74163, draw a circuit diagram and explain its working.

6. Write short notes on any three

i) Noise: Margins

ii) JTAG and BIST

iii) PAL and PLA

iv) Stuck at '0' and '1' faults

GN-Con.: 9117-14.