(Time: 3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is Compulsory.
       (2) Attempt any three questions out of remaining five.
       (3) Each question carries 20 marks and sub-question carry equal marks.
       (4) Assume suitable data if required.

Q1. a) Design and implement full subtractor using logic gates. (5)
     b) Explain the working of a two –inputs CMOS NOR gate with a neat Diagram. (5)
     c) Design a circuit using 2:1 MUX to implement 2 Input NAND Gate. (5)
     d) Evaluate following operation in BCD.
        (i) $(56)_{10} + (23)_{10}$  
        (ii) $(48)_{10} + (26)_{10}$  

Q2.a) Convert $(27)_{10}$ & $(42)_{10}$ into binary, octal, Hexadecimal, Excess-3 code and Gray code. (10)

     b) Draw a neat circuit diagram of four bit Twisted ring counter with initial state 0000 and relevant output waveforms. (10)

Q3.a) Design a combinational logic circuit with four input variables that will produce logic 1 output when input is greater than 9. (10)


     What is race around condition and how does it get eliminated ? (10)

Q4.a) Simplify the expression in POS form for given function and realize it with basic gates.

     \[ F(A,B,C,D) = \Sigma m (0,4,6,7,10,12,14) + d (2,13) \]  

     b) Convert the followings (10)
        i) SR flip flop to JK flip flop.  
        ii) JK flip-flop to D flip-flop

Q5 a) Implement the following expression using a single 8:1 multiplexer. (10)

     \[ F(A,B,C,D) = \Sigma m (0,2,4,6,8,10,12,14) \]

     b) Simplify the following four variable Boolean function using Quine-Mccluskey technique.
     \[ F(A, B, C, D) = \Sigma m (0, 2, 3,6,7,8,10,12,13) \]  

Q6.a) Design a Mod-5 synchronous up counter using T flip-flop. Design using minimal cost approach. (10)

     b) Explain interfacing of a TTL gate driving CMOS gates and vice versa. (10)