Q.P. CODE : 57445

MUMBAI UNIVERSITY

ELECTRONICS DEVICES & CIRCUITS-II

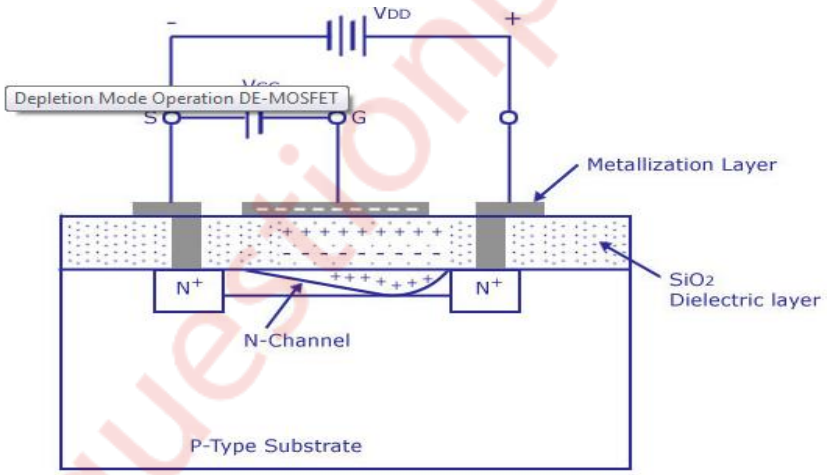
Semester 4 – MAY 19 – Choice Base

Q.1 Solve any four. **[20M]**

a) Draw and explain operation of depletion type MOSFET.

Ans : : i) MOSFET are metal oxide surface field effect transistor.There are two types of MOSFETS: depletion-type MOSFETs and enhancement-type MOSFETs.

ii) DE-MOSFET can be operated with either a positive or a negative gate. When gate is positive with respect to the source it operates in the enhancement—or E-mode and when the gate is negative with respect to the source, it operates in depletion-mode.



Depletion Mode Operation

iii) When the drain is made positive with respect to source, a drain current will flow, even with zero gate potential and the MOSFET is said to be operating in E-mode.

iv) In this mode of operation gate attracts the negative charge carriers from the P-substrate to the N-channel and thus reduces the channel resistance and increases the drain-current. The more positive the gate is made, the more drain current flows.

v) On the other hand when the gate is made negative with respect to the substrate, the gate repels some of the negative charge carriers out of the N-channel. This creates a depletion region in the channel, as illustrated in figure, and, therefore, increases the channel resistance and reduces the drain current.

vi) The more negative the gate, the less the drain current. In this mode of operation the device is referred to as a *depletion-mode MOSFET.* Here too much negative gate voltage can pinch-off the channel. Thus operation is similar to that of JFET.

b) Comapre RC coupled,TC coupled and DC coupled amplifier.

Ans :

No.	RC Coupled Amp.	TC Coupled Amp.	DC Coupled Amp.
1.	Resistor and capacitors Are coupling element in RC coupled amplifier.	Transformer is coupling Element in transformer coupled amplifier.	There is no element in Direct coupled amplifier.
2.	Impedance matching is Poor in RC coupled Amplifier.	Impedance matching is Excellent in TC coupled Amplifier.	Impedance matching is good In DC coupled amplifier.
3.	Frequency response is excellent at audio frequenc	Frequency response is poor.	Frquency response is good.
4.	It amplifies AC only.	It amplifies AC only.	It amplifies both AC as well as D DC.
5.	Application : Voltage or au amplifier.	Applicatiion : Power amplifier	Application : Low frequency Amplifier , OpAmp
6.	Size and cost is small.	It is having large and bulky size with cost.	Leat size and cost.

c)Explain design consideration of heat sinks in power amplifiers.

Ans : i) A suitable heat sink can now be selected. As the amount of power dissipation in the device increases, the size of the heat sink must increase to allow more surface area to be exposed to the ambient. First, the heat sink material and size are considered. Thermal conductivity of the material should be as high as possible.

ii) Copper is about the best for thermal conductivity and aluminum follows a close second. The difference in cost between copper and aluminum exceeds their difference in thermal

conductivity, therefore aluminum heat sinks are pretty much an industry standard. The ability of aluminum to conduct heat to the ambient is measured in °C/W of power dissipation, which primarily depends on its surface area and finish.

iii) Heat sinks are used for power transistors as the power dissipated at their collector junction is large. If heat dissipation is not done, this will cause large increases in junction temperature. In a transistor, the collector to base junction temperature (temperature of surrounding air) rises or because of self-heating.

iv) The self-heating is due to the power dissipated at collector junction This power dissipation at junction causes the junction temperature to rise, and this in turn increases the collector current which causes further increase in power dissipation. If the phenomenon continues then it may result in permanent damage of the transistor. This is known as thermal runaway.

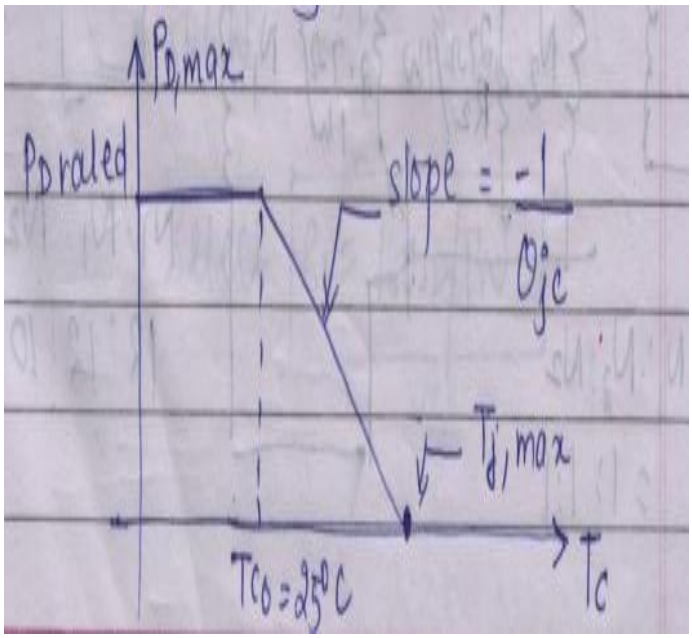
v) The temperature of the two types of power transistor is Germanium: 100°C to 110°C Silicon : 150°C to 200°C Heat sinks increase the power rating (ie. power handling capacity) of a transistor by getting rid of the heat developed quickly.

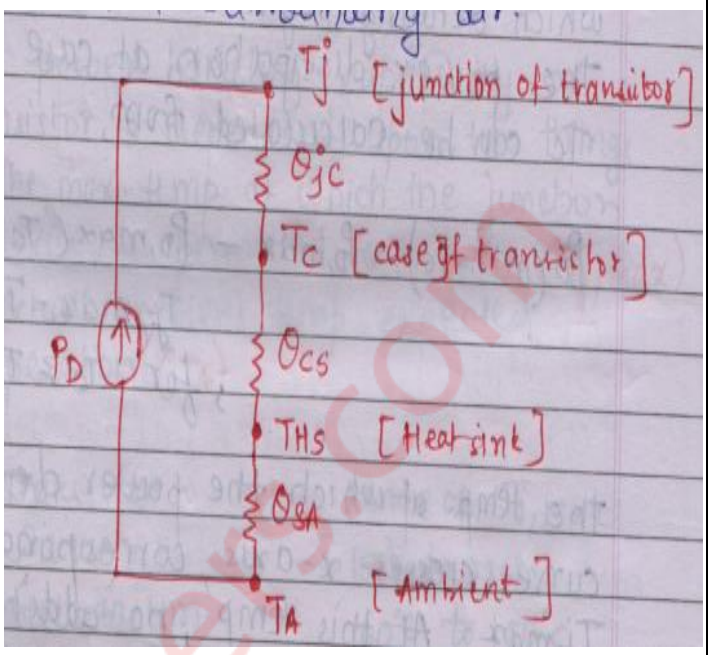
vi) It is in the form of a sheet of metal. Since the power dissipation within a transistor is mainly due to power dissipated at collector junction, the collector (connected to the case of the transistor) is bolted on to metal sheet for faster radiation of heat.

vii) Sometimes the transistor is connected to a large heat sink with fins causing more efficient removal of heat from the transistor. When heat flows out of a transistor, it passes through the case transistor and into the heat sink, which then radiates the heat into the surrounding air.

viii) The temperature of the transistor case T will be slightly higher than the temperature of the heat sink which in turn is slightly higher than the ambient temperature TA. Ambient Temperature: The heat produced at the junction passed through the transistor case (metal or plastic housing) are radiates to the surrounding air. The temperature of this air is known as the ambient temperature.

ix) Power derating curve : A plot of maximum rated power of device versuscase temperature of transistor is called as power derating curve of transistor.





d) Give the advantages of negative feedback.

Ans : i) Feedback is the process by which a fraction of the output signal, either a voltage or a current, is used as an input. If this feed back fraction is opposite in value or phase ("anti-phase") to the input signal, then the feedback is said to be Negative Feedback, or degenerative feedback.

ii)Negative feedback opposes or subtracts from the input signals giving it many advantages in the design and stabilisation of control systems.

iii) For example, if the systems output changes for any reason, then negative feedback affects the input in such a way as to counteract the change.

iv) Negative feedback also has effects of reducing distortion, noise, sensitivity to external changes as well as improving system bandwidth and input and output impedances.

v)The negative feedback reduces noise.It has highly stabilized gain.It can control step response of amplifier.

vi)It has less harmonic distortion.It has less amplitude distortion.It has less phase distortion.

vii)Input and output impedances can be modified as desired.It can increase or decrease output impedances.

viii) It has higher fidelity i.e. more linear operation.It has less frequency distortion.

e) State and explain Barkhausen's criteria.

Ans : i) Barkhausen's criterion states that,The loop gain is equal to unity in absolute magnitude, that is, | βA|=1|

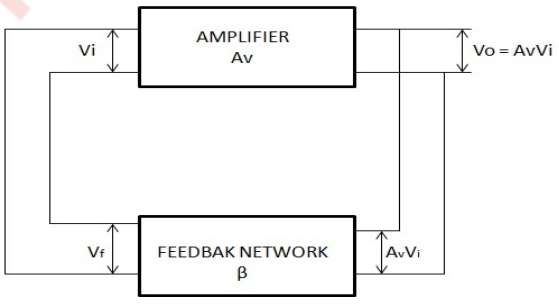
ii) βA| > 1: In this condition, feedback is greater than the input voltage Thus addition of input wave and feedback wave will result in larger amplitude wave and as oscillation goes on the amplitude will increase and this can be harmful for device.

iii) | βA| < 1: In this condition, feedback is less than the input voltage Thus addition of input wave and feedback wave will result in smaller amplitude wave and as oscillation goes on the amplitude will gradually decrease and oscillations will die out.

iv) | βA|=1, In this condition, feedback equal to the input voltage Thus addition of input wave and feedback wave will result wave having amplitude of input and as oscillation goes on the amplitude will remain constant and hence a sustained oscillation is achieved.

v) The phase shift around the loop is zero or an integer multiple of 2π. For phase shift equal to 180º | βA|=1 but input and feedback signal will be out of phase and they will cancel each other hence phase shift must be an integer multiple of 2π.

vi) An oscillator is an electronic circuit that generates sinusoidal oscillations known as sinusoidal oscillator. It converts input energy from a DC source into AC output energy of periodic waveform, at a specific frequency and is known amplitude. The characteristic feature of the oscillator is that it maintains its AC output.



vi) A sinusoidal oscillator is essentially a form of feedback amplifier, where special requirements are placed on the voltage gain Av and the feedback networks β.

vii) The oscillator ckt works on barkhauson's criteria, which states that an amplifier can be converted into an oscillator provided that following conditions must be satisfied.

--- Amplifier must have positive f/b

--- The Total Phase shift of the loop or circuit must be 3600 phase shift. The amplifier provides 1800 phase shift and the feedback network provides another 1800 phase shift. so the total phase shift of the circuit is 3600 phase shift.

--- | AB | ≥ 1 i.e. Loop gain value should be greater than or equal to one.

Q.2 a) Design a two stage RC coupled CE Amplifier to meet following specifications :

Av≥ $1000, Vo = 4V, S = 10, fL = 20Hz$. Select BC147B. **[15M]**

Ans : i) Given transistor is BC147B .The specifications of given transistor are :

V(CE,sat) = 0.25 V , hie =4.5K

hFE	200	290	450
hfe	240	330	500

ii) Selection of gains of first and second stage i.e Av' and Av''.

Av = 1000 i.e Av'.Av''=1000

Let Av' = 0.5(Av'')

Therefore , gain of first stage = Av' = 23 & gain of second stage = Av'' = 45 …(approx.)

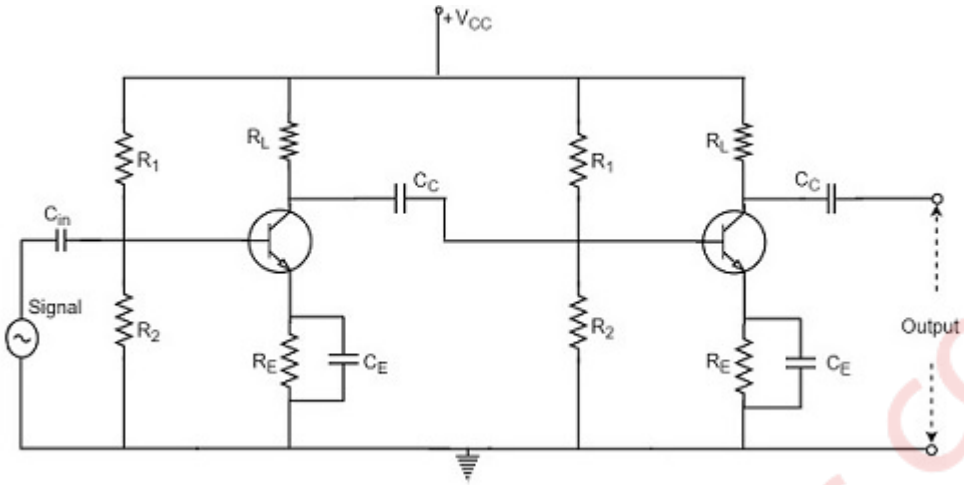
Now we know that , |Av''| = $\frac{hfe(min)\times Rc2}{hie}$

On solving , Rc2 = 1.5Kohms/(1/4)W

iii) Selection of Q point of second stage tx.

$$V(CEQ) \geq 1.5[Vo, peak + V(CE, sat)] \geq 1.5\left[4\sqrt{2} + 0.25\right] \geq 8.86\, V$$

Let V(CEQ) = 9 V



$$Ic(Q) \geq \frac{Vo,peak}{Rc2} \geq \frac{9}{1.5} \geq 3.77\ mA$$

Let $Ic(Q) = 4mA$ $\quad \therefore Q - point\ is\ (9V, 4mA)$

$$Vcc = 2.V(CEQ) = 2 * 9 = 18\ V$$

iv) Selection of RE2 : V(RE2) =Vcc – V(CEQ) – Ic(Q).Rc2 = 3 V

RE2 = V(RE2) / Ic(Q) = 3/4 = 0.75 ohms

RE2 = 820 ohms/(1/4)W

iv) Selection of R1 and R2 :

S = $1 + \frac{Rth}{RE} = 10$ => $\frac{Rth}{820} = 9$ => Rth = 7.6 KΩ

Vth - $\frac{Ic}{hFE}$ $.Rth - V(BE) - V(RE) = 0$

Vth = 2.38 V

But we know that using thevenins rule ,

Vth = $\frac{R2}{R1+R2}.Vcc$ & Rth = R1||R2

On solving this , we will get , R3 = 30K Ω / 0.25 W & R4 =11K Ω / 0.25W

v) Selection of Rc1 : Gain of first stage after considering load at output (Let RL)

Av' = $\frac{hfe(min) \times RL}{hie}$ $\quad => \quad RL = 750 \quad => Rc1\ ||Ri2 = 750$

Here Ri2 = R3||R4||hie = 2.79 Kohms

We will get Rc1 = 1.2 Kohms/0.25 W

vi) Selection of Q point of first stage tx.

$$V(CEQ) = \frac{Vcc}{2} = 9\ V$$

Let voltage across RE1 be 20% of Vcc . Therefore , V(RE1)=0.2(18) = 3.6 V

Henve V(Rc1)= Vcc – V(CEQ) – V(RE1) = 5.4 V

But Ic(Q).Rc1= 5.4 V => Ic(Q) = 4.5 mA

$$\therefore Q - point\ is\ (9V, 4.5mA)$$

$$Vcc = 2.V(CEQ) = 2 * 9 = 18\ V$$

vii) Selection of RE1 :

RE1= V(RE1) / Ic(Q) = 3.6/4.5 = 0.8 ohms

RE1 = 820 ohms/(1/4)W

viii) Selection of R1 and R2 :

S = 1 + $\frac{Rth}{RE}$ = 10 => $\frac{Rth}{820}$ = 9 = > Rth = 7.38 KΩ

Vth - $\frac{Ic}{hFE}$. $Rth - V(BE) - V(RE) = 0$

Vth = 2.6 V

But we know that using thevenins rule ,

Vth = $\frac{R2}{R1+R2}$. Vcc & Rth = R1||R2

On solving this , we will get , R1 = 27K Ω / 0.25 W & R2 =10K Ω / 0.25W

ix) Selection od coupling capacitors : fL= 20 Hz

fL(Cc1) = $\frac{1}{2\pi Req.Cc1}$ Req = Rs+Ri2 =2.78 Kohms

Cc1 = 2uF/10V

fL(Cc2) = $\frac{1}{2\pi Req.Cc2}$ Req = Rc1+R1||R2||hie = 0.6K + 27||10|| 250 = 4 Kohms

Cc1 = 2uF/10V

fL(Cc3) = $\frac{1}{2\pi Req.Cc3}$

Cc1 = 1.2mF/10V

x) Selection of CE1 AND CE2 :

fL(CE1) = $\frac{1}{2\pi Req.CE1}$ & fL(CE2) = $\frac{1}{2\pi Req.CE2}$

CE1 = 22uF/10V & CE2 = 22uF/10V

b) Explain the effect of source and load resistance on amplifier. [5M]

Ans : i) The input impedance of an amplifier is the input impedance "seen" by the source driving the input of the amplifier. If it is too low, it can have an adverse loading effect on the previous stage and possibly affecting the frequency response and output signal level of that stage. But in most applications, common emitter and common collector amplifier circuits generally have high input impedances.

ii) V_S is the signal voltage, R_S is the internal resistance of the signal source, and R_L is the load resistance connected across the output.When an amplifier is connected to a signal source, the source "sees" the input impedance, Zin of the amplifier as a load.

iii) Likewise, the input voltage, Vin is what the amplifier sees across the input impedance, Zin. Then the amplifiers input can be modelled as a simple voltage divider circuit

iv) When a load resistance, RL is connected to the output of the amplifier, the amplifier becomes the source feeding the load. Therefore, the output voltage and impedance automatically becomes the source voltage and source impedance for the load.

v)The input impedance may depend upon the source supply feeding the amplifier while the output impedance may also vary according to the load impedance, RL across the output terminals.

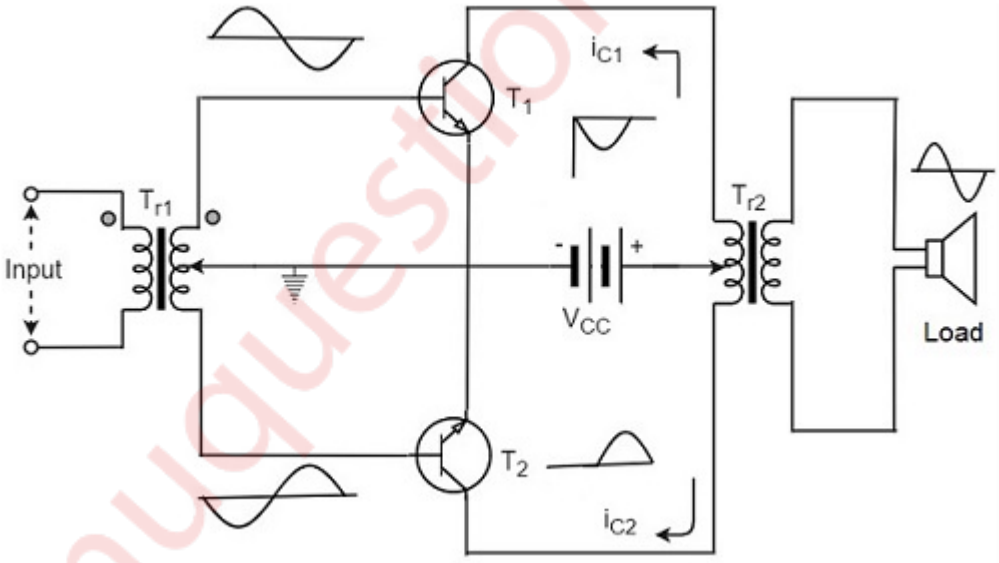
Q.3 a) Draw circuit diagram of Class B push pull power amplifier and explain its working.Find its maximum efficiency and maximum power dissipation in each transistor.What is cross over distortion ? How it can be overcome ?. [10M]

Ans : i) When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as class B power amplifier.

ii) The biasing of the transistor in class B operation is in such a way that at zero signal condition, there will be no collector current. The operating point is selected to be at collector cut off voltage. So, when the signal is applied, only the positive half cycle is amplified at the output.

iii)Class B Push Pull Power Amplifier : - Though the efficiency of class B power amplifier is higher than class A, as only one half cycle of the input is used, the distortion is high. Also, the input power is not completely utilized. In order to compensate these problems, the push-pull configuration is introduced in class B amplifier.

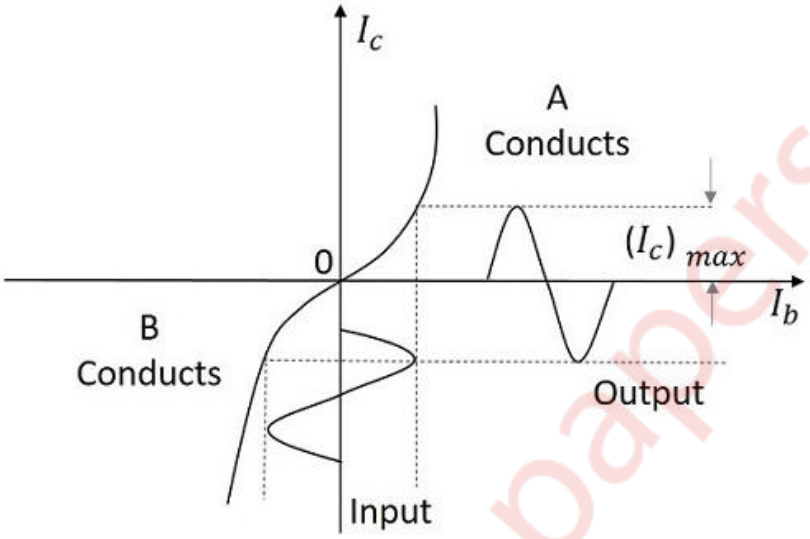
iv) The circuit of a push-pull class B power amplifier consists of two identical transistors T1 and T2 whose bases are connected to the secondary of the center-tapped input transformer Tr1. The emitters are shorted and the collectors are given the VCC supply through the primary of the output transformer Tr2.



v) The circuit arrangement of class B push-pull amplifier, is same as that of class A push-pull amplifier except that the transistors are biased at cut off, instead of using the

biasing resistors. The figure below gives the detailing of the construction of a push-pull class B power amplifier.

vi) The circuit of class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors T1 and T2 are in cut off condition and hence no collector currents flow. As no current is drawn from VCC, no power is wasted.



vii) When input signal is given, it is applied to the input transformer Tr1 which splits the signal into two signals that are 180o out of phase with each other. These two signals are given to the two identical transistors T1 and T2. For the positive half cycle, the base of the transistor T1 becomes positive and collector current flows. At the same time, the transistor T2 has negative half cycle, which throws the transistor T2 into cutoff condition and hence no collector current flows. The waveform is produced as shown in the following figure.

viii)For the next half cycle, the transistor T1 gets into cut off condition and the transistor T2 gets into conduction, to contribute the output. Hence for both the cycles, each transistor conducts alternately. The output transformer Tr3 serves to join the two currents producing an almost undistorted output waveform.

ix) Power Efficiency of Class B Push-Pull Amplifier : The current in each transistor is the average value of half sine loop.

$$I(dc) = \frac{Ic.max}{\pi}$$

$$Pin(dc) = 2 \times \left[\frac{Ic.max}{\pi} \times Vcc\right]$$

Here factor 2 is introduced as there are two transistors in push-pull amplifier.

x) R.M.S. value of collector current = Ic.max/$\sqrt{2}$
R.M.S. value of collector current = Vcc/$\sqrt{2}$
Under ideal conditions of maximum power,

Po(ac) =(Ic.max)(Vcc)/2

Now overall maximum efficiency , $\eta(\text{overall}) = \frac{Po(ac)}{Pin(DC)} = \frac{Ic(max)\times Vcc}{2} \times \frac{\pi}{2\times Ic(max)\times Vcc}$

$\therefore \quad \eta(\text{overall}) = \frac{\pi}{4} = 0.785$

Hence overall efficiency of class B push pull power amplifier is 78.5%.

xi) Cross-over distortion : Crossover Distortion is a common feature of Class-B amplifiers where the non-linearities of the two switching transistors do not vary linearly with the input signal.

xii) Crossover Distortion produces a zero voltage “flat spot” or “deadband” on the output wave shape as it crosses over from one half of the waveform to the other. The reason for this is that the transition period when the transistors are switching over from one to the other, does not stop or start exactly at the zero crossover point thus causing a small delay between the first transistor turning “OFF” and the second transistor turning “ON”. This delay results in both transistors being switched “OFF” at the same instant in time.

xiii) Overcome cross over distortion : The problem of Crossover Distortion can be reduced considerably by applying a slight forward base bias voltage (same idea as seen in the Transistor tutorial) to the bases of the two transistors via the center-tap of the input transformer, thus the transistors are no longer biased at the zero cut-off point but instead are “Pre-biased” at a level determined by this new biasing voltage

b) Draw and explain Cascode amplifier in detail. **[10M]**

Ans : i)Cascode amplifier is the two stage amplifier in which common emitter stage is connected to common base stage. The input signal is applied at Q1 i.e at common emitter stage and output is obtained at Q2.

ii)A common-base configuration is not subject to the Miller effect because the grounded base shields the collector signal from being fed back to the emitter input. Thus, a C-B amplifier has better high frequency response. The way to reduce the common-emitter gain is to reduce the load resistance.

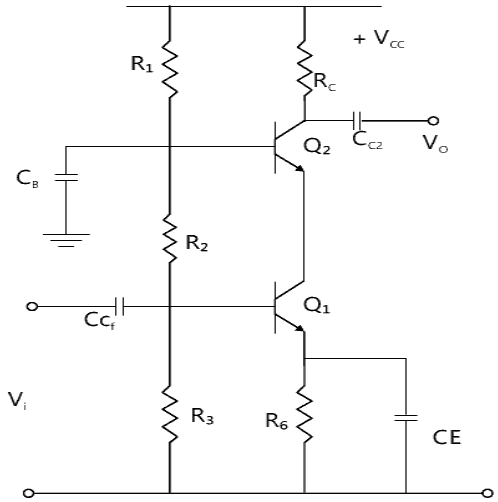
iii)The gain of a C-E amplifier is approximately Rc/R e. The collector load Rc is the resistance of the emitter of the C-B stage loading the C-E stage. CE gain amplifier gain is approximately Av = Rc/Re=1. This Miller capacitance is Cmiller = Ccbo(1-Av) = Ccbo (1-(-1)= 2 Ccbo. Cascode amplifier 15 Ccbo (1-(-1)= 2 Ccbo. We now have a moderately high input impedance C-E stage without suffering the Miller effect, but no C-E stage voltage gain. The C-B stage provides a high voltage gain.

iv)The total current gain of cascode is β as current gain of the C-E stage is 1 for the C-B is β. A cascode amplifier has a high gain, moderately high input impedance, a high output impedance, and a high bandwidth.

v)The cascode is a two-stage amplifier composed of a single transconductance amplifier (usually a common source/emitter stage) followed by a current follower (usually a common gate/base stage).

vi) Compared to a single amplifier stage, this combination may have one or more of the following advantages: higher input-output isolation, higher input impedance, higher output impedance, higher gain or higher bandwidth. In modern circuits, the cascode is often constructed from two transistors (BJTs or FETs), with one operating as a common emitter/source and the other as a common base/gate.

vii)The cascode improves input-output isolation (or reverse transmission) as there is less direct coupling from the output to input. This greatly reduces the Miller multiplication of stray coupling capacitance between input and output and thus contributes to a much higher bandwidth.



CASCODE amplifier

viii) The advantage of the cascode configuration stems from the placement of an upper transistor as the load of the input transistor's output terminal (collector / drain). This upper transistor is referred to as the cascode device. Because at high frequencies the cascode transistor's base/gate is effectively grounded by DC voltage source VBias, the cascode device's emitter / source voltage (and therefore the lower input transistor's collector / drain) is held at a more constant voltage during operation. In other words, the cascode device exhibits a low input resistance to the lower transistor, making the voltage gain seen at the collector / drain of the lower device very small, which dramatically reduces the Miller feedback capacitance from the lower transistor's collector to base or drain to gate.

ix)This loss of voltage gain is recovered by the cascode transistor. Thus, the cascode transistor permits the lower common emitter / source stage to operate with minimum negative (Miller) feedback, improving the bandwidth of the overall amplifier.

x) The base or gate of the cascode device is electrically AC grounded, so charge and discharge of stray capacitance Ccb or Cdg between collector and base or drain and gate is simply through RL the output load, and the frequency response is affected only for frequencies above the associated RC time constant: In the case of a FET device t = Cdg RD||Rout, a rather high frequency because Cdg is small. That is, the upper FET gate does not suffer from Miller multiplication of Cdg.

xi) If the cascode device stage were operated alone using its emitter or source as input node (i.e. common base/gate configuration), it would have good voltage gain and wide bandwidth. However, its low input impedance would limit its usefulness to very low

impedance voltage drivers. Adding the lower common emitter/source stage results in an increased input impedance, allowing the cascode stage to be driven by a higher impedance source.

xii) If one were to replace the upper device with a typical resistive load, and take the output from the input transistor's collector or drain the common emitter/source configuration would offer the same input impedance as the cascode configuration, but the cascode configuration would offer a potentially greater gain and much greater bandwidth.

Q.4 a) Design a class A transformer coupled power amplifier for the following requirements.

Output A.C power = 5 watts,Load resistance=12ohms,DC supply voltage=12 V

S(ICO)≤ 8 . Calculate overall efficiency at full load. **[10M]**

Ans : i) Power to be delivered across primary Po(ac) = PL' = $\frac{PL}{nT}$

Let efficiency of transformer be 80%. Hence Po(ac) = $\frac{5}{0.8} = 6.25\ W$

ii) Selection of transistor Pd(max) $\geq 2Po(ac) = 12.5\ W$

Select ECN149 having following specification PD(max) =30W , Ic(max) =4A,V(CE sat) = 1V

V(BE max) = 1.2 V , V(CE max) = 40 , hFE(typ)=50

iii) Now DC supply voltage is 12 V.

Voltage across RE is V(RE) == 10 %.Vcc = 1.2 V

iv) To find Q point : V(CEQ) = Vcc – V(RE) = 12 – 1.2 = 10.8 V

Vo(p) = V(CEQ) – V(CEsat) = 10.8 – 1 = 9.8 V

Vm = Vo(p) = 9.8 V

Io(p) = Ic(Q) $\geq \frac{Vo(p)}{RL'}$

v) Calculation Of RL' : Po(ac) = $\frac{Vm.Im}{2} = \frac{Vm^2}{2RL'} \Rightarrow RL' = \frac{Vm^2}{2.Po(ac)} = 7.7\ ohms$

Now , RL' = $(\frac{N1}{N2})^2.RL \Rightarrow \frac{N1}{N2} = \sqrt{\frac{RL'}{RL}} = \sqrt{\frac{7.7}{12}} = 0.80$

Ic(Q) $\geq \frac{Vo(p)}{RL'} \geq \frac{9.8}{7.7} \geq 1.2727\ A$

Let Ic(Q) = 1.3 A

Now , RE = $\frac{V(RE)}{Ic(Q)} = \frac{1.2}{1.3} = 0.92\ ohms$

P(RE) = $Ic(Q)^2.RE = 0.92(1.3 * 1.3) = 1.55\ W$

Select RE ,LSV so that power dissipation in terms of heat is less and efficiency is more.

Hence RE = 0.9 ohms / 2W

vi) To Find R1 & R2 : -

S = 1 + $\frac{Rth}{RE}$ = 10 => $\frac{Rth}{0.9}$ = 9 => Rth = 8.1 Ω

Vth - $\frac{Ic}{hFE}$ $.Rth - V(BE) - V(RE) = 0$

Vth = 2.11 V

But we know that using thevenins rule ,

Vth = $\frac{R2}{R1+R2}.Vcc$ & Rth = R1||R2

On solving this , we will get , R1 = 46 Ω / 3 W & R2 = 9 Ω / 3W

vii) Selection of transformer : Select transformer with turn's ratio of 0.8:1 and having primary current Ip$\geq 2Ic(Q) \geq 2.6A$

vii) Selection of capacitors : Assume fL=50 Hz

fL(Cei) = $\frac{1}{2\pi Req.Cei}$ Req = Rth||hie = 8.1 || 250 = 7.845 ohms

Cei = 40 mF / 12V

fL(CE) = $\frac{1}{2\pi Req.CE}$ Req = 0.1 RE = 0.09

CE = 36 mF / 12 V

viii) Full load efficiency : Po(ac FL) = $\frac{Vm.Im}{2} = \frac{9.8\times1.3}{2} = 6.37\ W$

P(dc) = Vcc.Ic(Q) + $\frac{Vcc\times Vcc}{R1+R2} = 12(1.3) + \frac{12\times12}{55} = 19\ W$

Assumed efficiency is 80%.

$$nT = \frac{PL(FL)}{Po,ac(FL)} = \frac{PL(FL)}{6.37} = 0.8$$

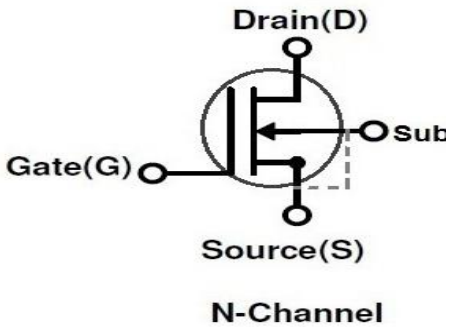
PL(FL)= 5.096 W

Efficiency at full load = $n(FL) = \frac{PL(FL)}{PDC} = \frac{5.096}{19} = 0.26$

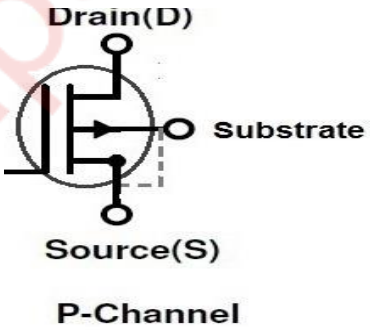
Hence efficiency at full load is 26%.

b) Explain the different types of biasing of Depletion MOSFET. [10M]

Ans : i) The depletion type MOSFET transistor is equivalent to a "normally closed" switch. The depletion type of transistors requires gate – source voltage (V_{GS}) to switch OFF the device.



N-Channel



P-Channel

ii) The symbols for depletion mode of MOSFETs in both N-channel and P-channel types are shown above. In the above symbols we can observe that the fourth terminal substrate is connected to the ground, but in discrete MOSFETs it is connected to source terminal.

iii) The continuous thick line connected between the drain and source terminal represents the depletion type. The arrow symbol indicates the type of channel, such as N-channel or P-channel. In this type of MOSFETs a thin layer of silicon is deposited below the gate terminal. The depletion mode MOSFET transistors are generally ON at zero gate-source voltage (V_{GS}).

iv)The conductivity of the channel in depletion MOSFETs is less compared to the enhancement type of MOSFETs.

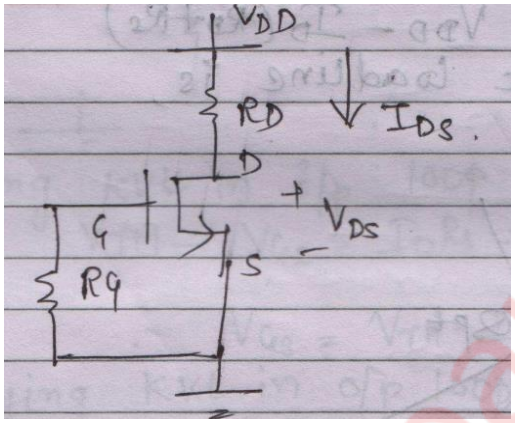
v) The various biasing circuits for D- MOSFET are :

-- Zero Biasd Circuit

-- Self Biasd

-- Voltage Divider Biased

vi) Zero Bias : In this biasing technique , Vg = 0 as Ig = 0 and V(GS) = 0V and V(DS)=V(DD)-ID.RD



vii) Self Biased :

Apply KVL in I/P loop,

-V(GS)-ID.RS = 0

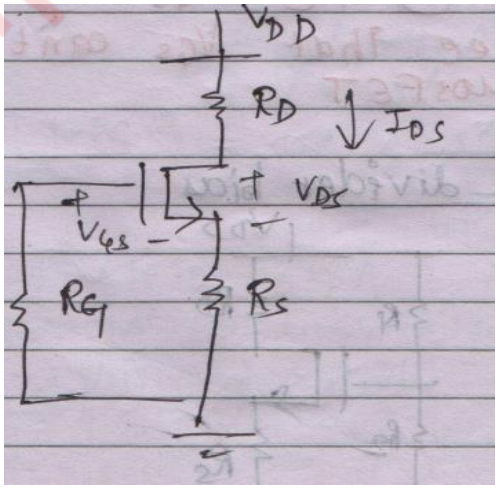
-V(GS) = ID.RS

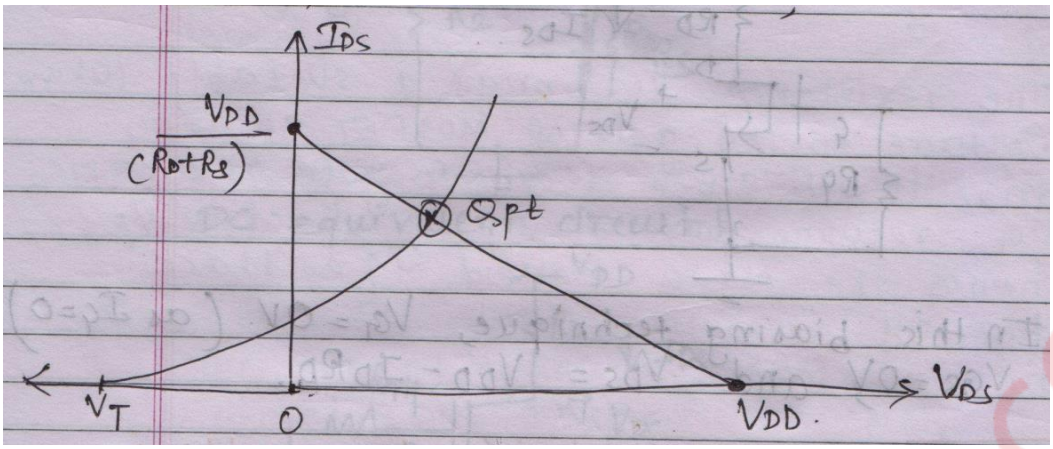
Apply KVL in O/P loop ,

V(DD)-ID.RD-V(DS)-ID.RS = 0

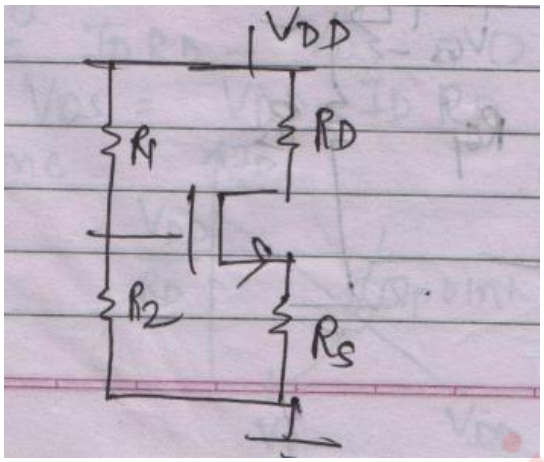
V(DD)-ID.RD-ID.RS = V(DS)

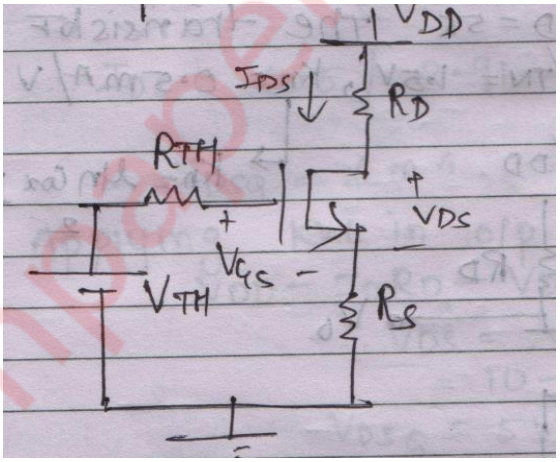
DC loadline is shown below.





viii) Voltage divider biased : Voltage divider bias circuit with its Thevenins equivalent circuit is :





V(TH)= $\frac{R2}{R1+R2}.Vdd$ & R(TH)= R1 || R2

Applying KVL in i/p loop ,

V(TH) – V(GS) – ID.RS = 0

∴ V(TH) – ID.RS = V(GS)

Applying KVL in o/p loop,

Vdd – ID.RD –V(DS) –ID.RS = 0

∴ Vdd – ID.RD –ID.RS = V(DS)

Q.5 a) Explain the different feedback topologies in detail. [15M]

Ans : i) The feedback-amplifier can be defined as an amplifier which has feedback lane that exists between o/p to input. In this type of amplifier, feedback is the limitation which calculates the sum of feedback given in the following amplifier.

ii) The feedback factor is the ratio of the feedback signal and the input signal.

iii) The procedure of introducing some device's output energy fraction from back to the i/p is termed as Feedback. This is mainly used to reduce the noise as well as to make the operation of an amplifier is constant.

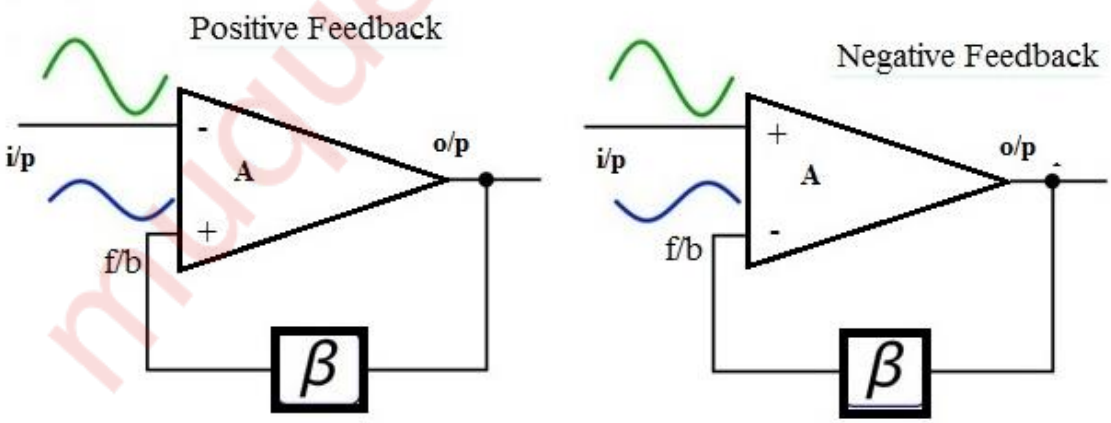
iv) This amplifier can be classified into two types based on the feedback signal helps such as positive & negative feedback amplifier.

1) Positive Feedback Amplifier

The positive feedback can be defined as when the feedback current otherwise voltage is applied for increasing the i/p voltage, then it is named as positive feedback. Direct feedback is another name of this positive feedback. Because positive feedback generates unnecessary distortion; it is not often used in amplifiers. But, it amplifies the original signal power and can be used in oscillator circuits.

2) Negative Feedback Amplifier

The negative feedback can be defined as if the feedback current otherwise voltage can be applied for reducing the amplifier i/p, then it is called as negative feedback. Inverse feedback is another name of this negative feedback. This kind of feedback is regularly used in amplifier circuits.



v) **Feedback Amplifier Topologies**

There are four basic amplifier topologies for connecting the feedback signal. Both the current as well as voltage can be feedback toward the input in series otherwise in parallel.

---Voltage Series Feedback Amplifier

---Voltage Shunt Feedback Amplifier

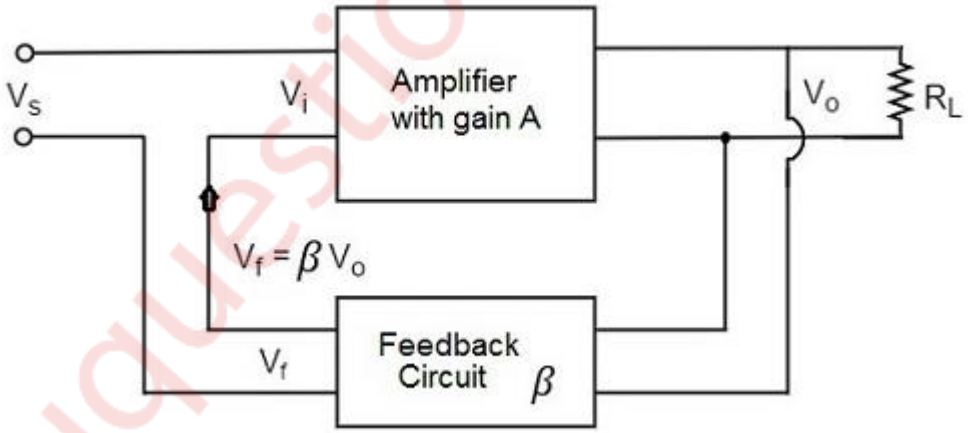
---Current Series Feedback Amplifier

---Current Shunt Feedback Amplifier

a) Voltage Series Feedback Amplifier

In this type of circuit, a portion of the o/p voltage can be applied to the input voltage in series through the feedback circuit. The block diagram of the voltage series feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output although in series by means of the input.

When the feedback circuit is allied in shunt through the output, then the o/p impedance will be reduced and the i/p impedance is enlarged because of the series connection with the input.

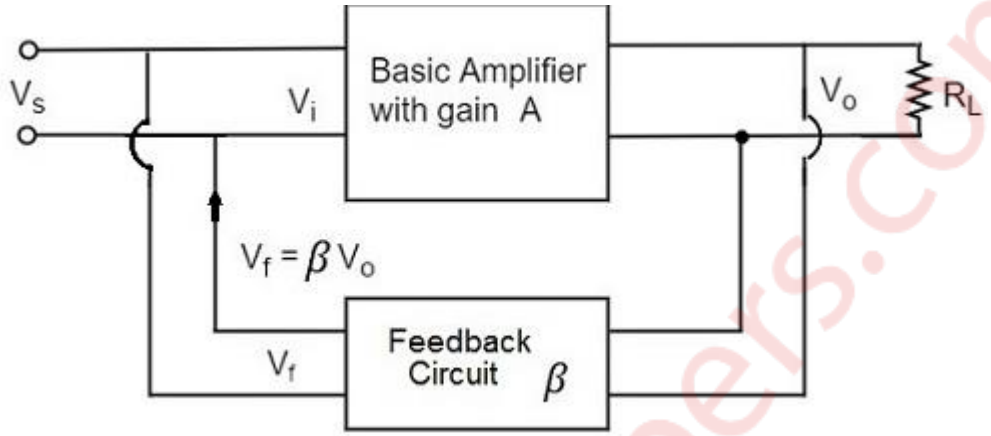


b) Voltage Shunt Feedback Amplifier

In this type of circuit, a portion of the o/p voltage can be applied to the input voltage in parallel with through the feedback circuit. The block diagram of the voltage shunt

feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output as well as the input.

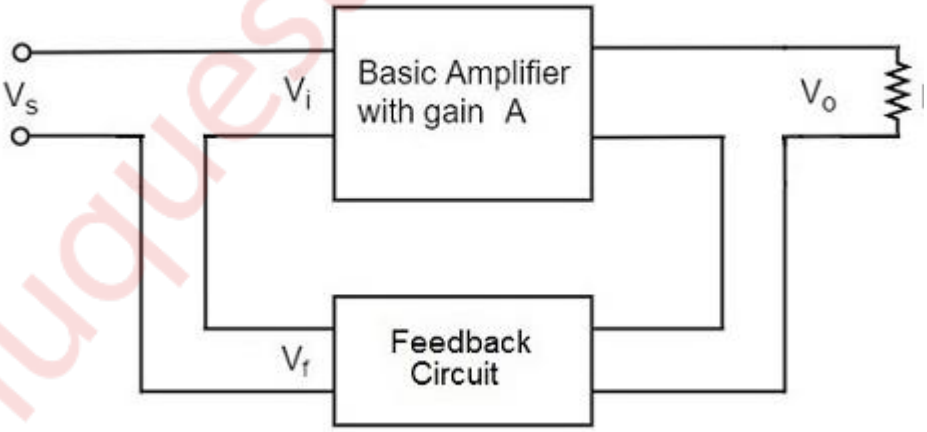
When the feedback circuit is allied in shunt through the o/p as well as the input, then both the o/p impedance & the i/p impedance will be decreased.



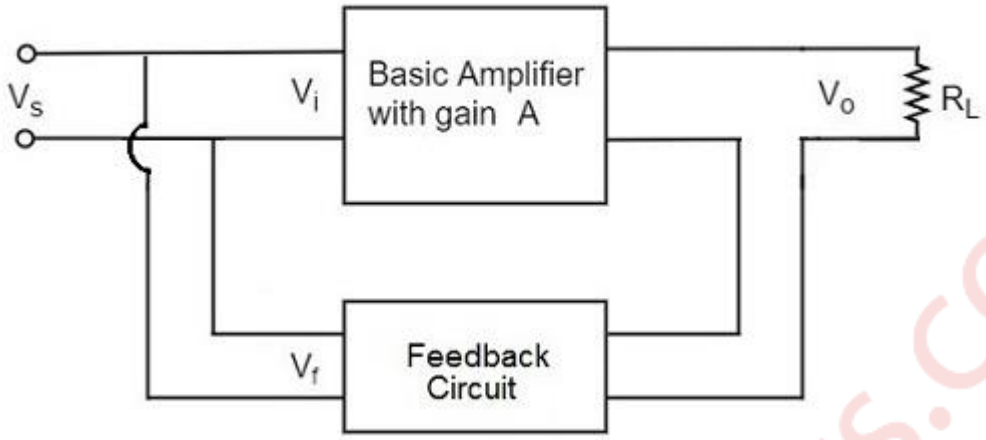
c) Current Series Feedback Amplifier

In this type of circuit, a portion of the o/p voltage is applied to the i/p voltage in series through the feedback circuit. The block diagram of the current series feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in series by means of the output as well as the input.

When the feedback circuit is allied in series through the o/p as well as the input, then both the o/p impedance & the i/p impedance will be increased.



d) Current Shunt Feedback Amplifier :



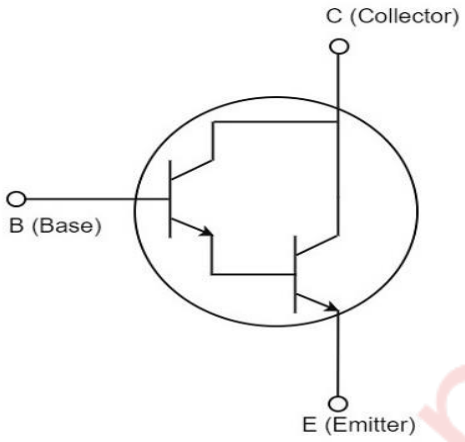
In this type of circuit, a portion of the o/p voltage is applied to the i/p voltage in shunt through the feedback circuit. The block diagram of the current shunt feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output as well as the input.

When the feedback circuit is allied in series through the o/p however in parallel with the input, then the o/p impedance will be increased & because of the parallel connection with the i/p, the i/p impedance will be decreased.

Feedback Topology	Input Resistance	Output Resistance
Voltage Series	Increases Rif = Ri*(1+A*β)	Decreases Rof=Ro/(1+A*β)
Current Series	Increases Rif = Ri*(1+A*β)	Increases Rof = Ro*(1+A*β)
Current Shunt	Decreases Rif = Ri/(1+A*β)	Increases Rof = Ro*(1+A*β)
Voltage Shunt	Decreases Rif = Ri*(1+A*β)	Decreases Rof=Ro/(1+A*β)

b) Write short notes on Darlington pair amplifier. [5M]

Ans : i) Darlington pair, contains of two BJTs that are connected to deliver a high current gain from a low base current. In this transistor, the emitter of the i/p transistor is connected to the o/p of the base of the transistor and the collectors of the transistor are wired together.



ii) So, the i/p transistor amplifies the current even further amplifies by the o/p transistor. Darlington transistors are classified into different types by Power Dissipation, Max CE Voltage, Polarity, Min DC Current Gain and type of Packaging.

iii)The common values of max CE voltage are 30V, 60V, 80V & 100V. The max CE voltage of Darlington transistor is 450V and power dissipation can be in the range of 200mW to 250mW.

iv) The following are the important characteristics of Darling ton amplifier.

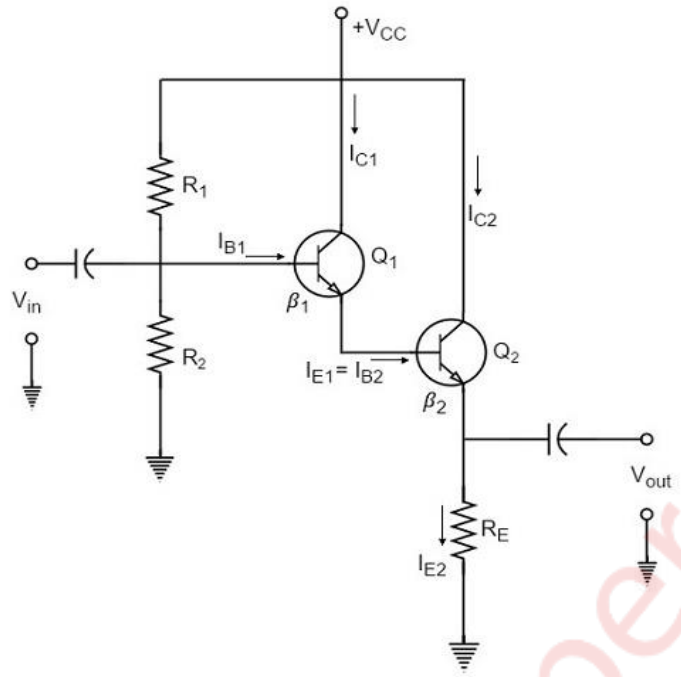
---Extremely high input impedance (MΩ).

---Extremely high current gain (several thousands).

---Extremely low output impedance (a few Ω).

v) The emitter follower circuit which was just discussed lacks to meet the requirements of the circuit current gain (A_i) and the input impedance (Z_i).

vi) In order to achieve some increase in the overall values of circuit current gain and input impedance, two transistors are connected as shown in the following circuit diagram, which is known as Darlington configuration.



∴ Ic=Ic1+Ic2

∴ Ic= β1.IB+ β2.IB2

vii) But the base current of the transistor Q1 is equal to IE1(emitter current), and emitter of the TR1 transistor is connected to the base terminal of the transistor Q2.

IB2 = IE1
= Ic1+ IB
= β1.IB +IB
= IB(β1 + 1)

Substitute this IB2 value in the above equation

∴ Ic= β1.IB+ β2. IB(β1 + 1)

∴ Ic= β1.IB + β2. IB β1 + β2. IB

∴ Ic= (β1+ (β2.β1) + β2). IB

In the above equation, β1 and β2 are gains of individual transistors.

vii) Here, the overall current gain of the first transistor is multiplied by the second transistor that is specified by β, & a couple of bipolar transistors are combined to form a single Darlington transistor with a very high i/p resistance and value of β.

viii) Darlington Transistor Applications :

This transistor is used in various applications where a high gain is required at a low frequency. Some applications are :

---Power Regulators

---Audio Amplifier o/p stages

---Controlling of motors

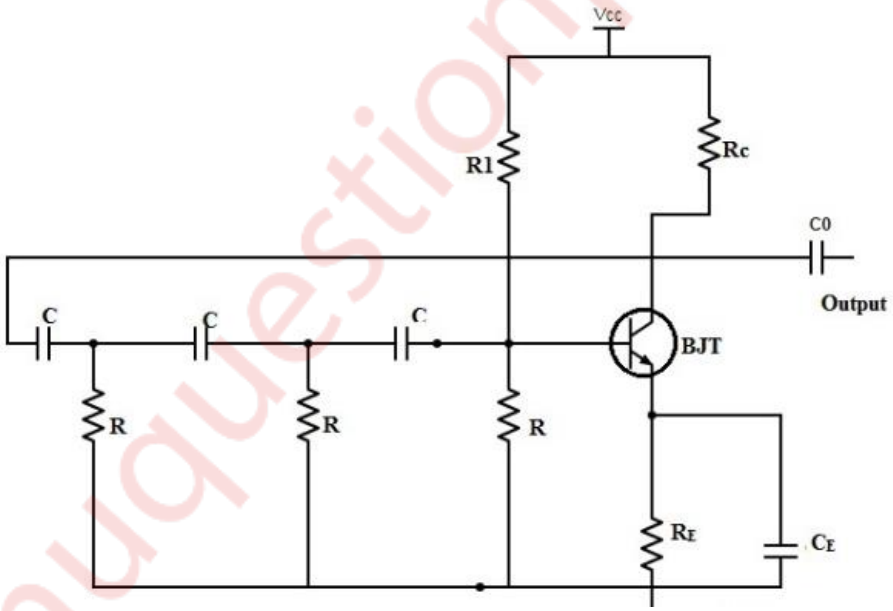
---Display drivers

---Controlling of Solenoid

---Light and touch sensors.

Q.6 a) Draw RC phase shift oscillator using BJT and derive the frequency of oscillation for same. [15M]

Ans : i) The following RC phase shift oscillator circuit using BJT can be built by cascading 3-RC phase shift networks; each provides a 60deg. phase shift. In the circuit, the RC which is known as the collector resistor stops the transistor's collector current.



ii) The resistor which is near to the transistors like R & R1 can form the voltage divider circuit as the RE (emitter resistor) develops the strength. After that, the two capacitors namely Co & CE, where Co is the o/p DC decoupling capacitor & CE is the emitter bypass

capacitor correspondingly. Further, this circuit also demonstrates 3-RC networks used within the feedback path.

iii) This connection will cause the o/p waveform to move with 180deg. throughout its journey from o/p terminal toward the transistor's base terminal.

iv) After that, this signal can be moved once more with 180deg. with the help of the transistor within the network because of the truth that the phase disparity among the input as well as the output can be 180 deg. in the common emitter (CE) configuration. This will create the network phase disparity to 360 degrees and satisfies the phase disparity condition.

v) Derivation for frequency of oscillations :

$$-I1.Rc - \frac{1}{j.w.c}I1 - (I1 - I2)R - hFE.Ib.Rc = 0$$

$$-I1.Rc - \frac{1}{j.w.c}I1 - (\ I1).R + (I2)R = hFE.Rc.Ib$$

$$(\ hFE.Rc.Ib\ + (I2)R = I1[Rc + \frac{1}{j.w.c} + R] \quad \text{.....(1)}$$

$$-(I2 - I1)R - \frac{1}{j.w.c}I2 - (I2 - I3)R = 0$$

$$I1.R - I2\left[2R + \frac{1}{j.w.c}\right] + I3.R = 0 \quad \text{.....(2)}$$

$Similarly,$

$$I2.R - I3\left[2R + \frac{1}{j.w.c}\right] = 0 \quad \text{.....(3)}$$

Let $\alpha = \frac{1}{w.Rc}$ and k=$\frac{Rc}{R}$

Get I1,I2 in terms of I3.

From equation 3 after dividing by R,

$$I2 = I3[2 - j.\alpha]$$

$From\ equation\ 2$,

$$I1 = I3[3j.4.\alpha - \alpha^2]$$

Substitute in equation 1,we will get ,

$$-hFE.k.Ib = I3[1 + 3.k - (5 + k)\alpha^2 - j(6\alpha + 4\alpha k - \alpha^3)]$$

$$Now\ , \frac{I3}{Ib} = \frac{-hFE.k}{[1 + 3.k - (5 + k)\alpha^2 - j(6\alpha + 4\alpha k - \alpha^3)]}$$

Loop gain is always real , $6\alpha + 4\alpha k - \alpha^3 = 0$

$$6 + 4k = \alpha^2$$

$$\alpha = \frac{1}{w.R.C}$$

Squaring we will get , $w^2 = \frac{1}{(6+4k)R^2C^2}$ but w= $2\pi f$

Hence , $f = \frac{1}{2\pi R.C\sqrt{(6+4k)}}$ where k= $\frac{Rc}{R}$

For sustained oscillations , $\frac{I3}{Ib} > 1$ $\therefore$ $hFe > 4k + 23 + \frac{29}{k}$

vi) The advantages of this phase shift oscillator include the following :

---The oscillator circuit designing is easy with basic components like resistors as well as capacitors.

---This circuit is not expensive and gives excellent frequency stability.

---These are mainly suitable for low-frequencies

---This circuit is simpler compared with a Wein bridge oscillator because it doesn't require the stabilization planning & negative feedback.

---The circuit output is sinusoidal that is somewhat distortion free.

---The frequency range of this circuit will range from a few Hz to hundreds of kHz

vii) Disadvantages of RC-Phase Shift Oscillator : -

---The disadvantages of this phase shift oscillator include the following.

---The output of this circuit is small because of the smaller feedback

---It requires 12 volts battery for developing a suitably huge feedback voltage.

---It is hard for this circuit to create oscillations because of the small feedback

---The frequency stability of this circuit is not good to compare with Wien bridge oscillator.

viii) RC Phase Shift Oscillator Applications :-

---The applications of this type of phase shift oscillator include the following

---This phase shift oscillator is used to generate the signals over an extensive range of frequency. They used in musical instruments, GPS units, & voice synthesis.

---The applications of this phase shift oscillator include voice synthesis, musical instruments, and GPS units.

b) For Hartley oscillator calculate the frequency of oscillation if L1=L2=1mH and C = 0.2uF.

[5M]

Ans : Given : L1 = L2 = 1mH , C = 0.2 μF

To Find : Frequency of oscillations for hartley oscillator = f = ?

Formula : $\boldsymbol{f_r = \frac{1}{2\pi\sqrt{L.C}}}$, **L = L1 + L2**

Solution : We know that the frequency of oscillations for Hartley oscillator is ,

$$f = \frac{1}{2\pi\sqrt{(L1+L2).C}}$$

$$\therefore f = \frac{1}{2\pi\sqrt{(1m+1m).(0.2\mu)}}$$

$$\therefore \boldsymbol{f = 7.96\ KHz}$$