ME ELX SEM-II (CBCGS) Sub - DDRA DT 17-5-2017

QP Code : 13829

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **three** questions out of **remaining five**.
(3) **Each** question carries **20** marks and sub-questions carry **equal** marks.
(4) Assume suitable **data** if required.

1. (a) Draw the state diagram for non-overlapping sequence "1100". **5**
   (b) What is the difference between signal and variable. **5**
   (c) Explain various elements used in ASM charts. **5**
   (d) Explain the clock management used in FPGA. **5**

2. (a) For the given logic diagram in Figure 1 below, draw the state diagram **10**

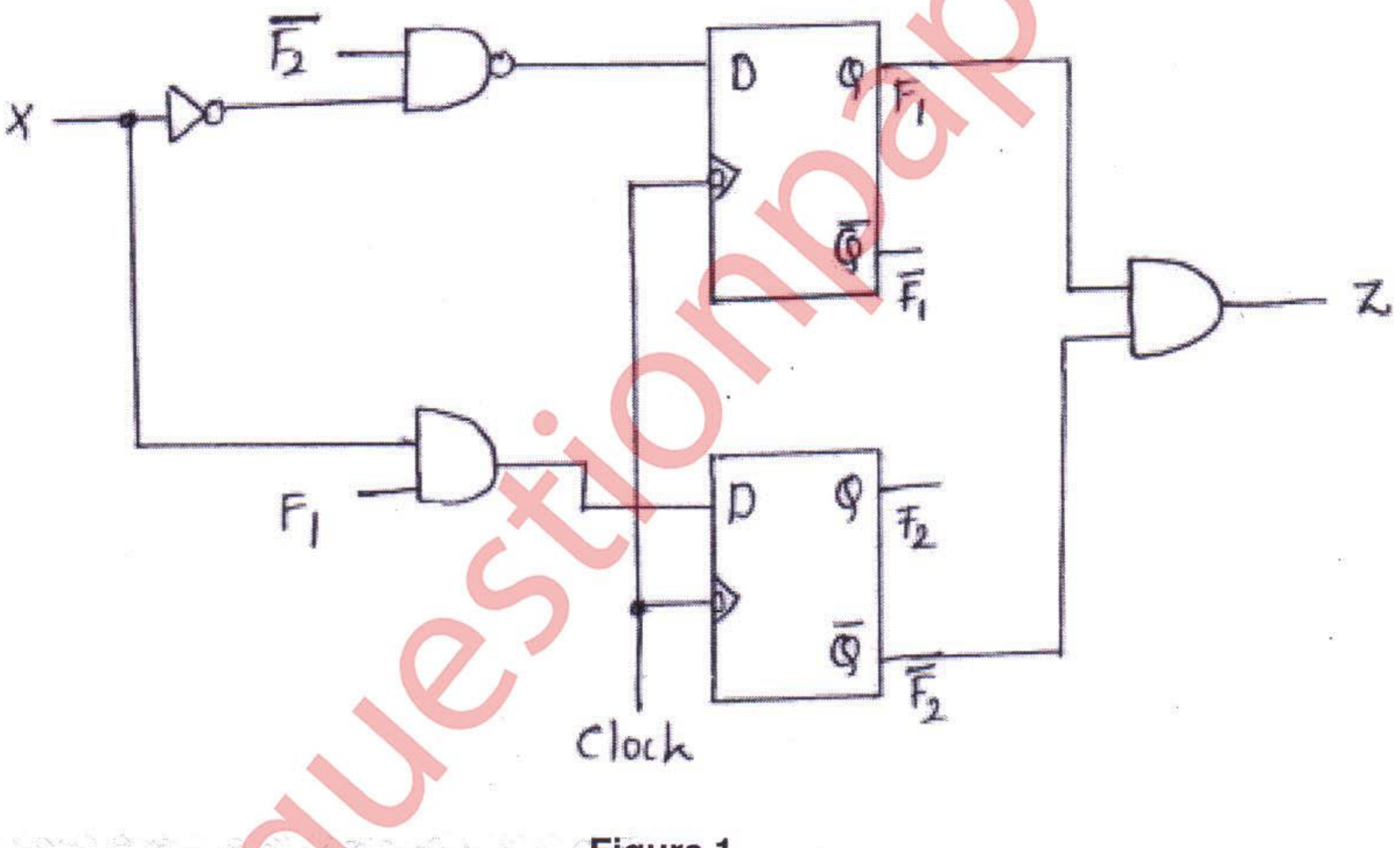

Figure 1

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(b) A state diagram of a sequential machine is shown in Figure 2 below. Recognize the type of machine. Identify the redundent state. Obtain the simplified state diagram. Also design the machine. **10**

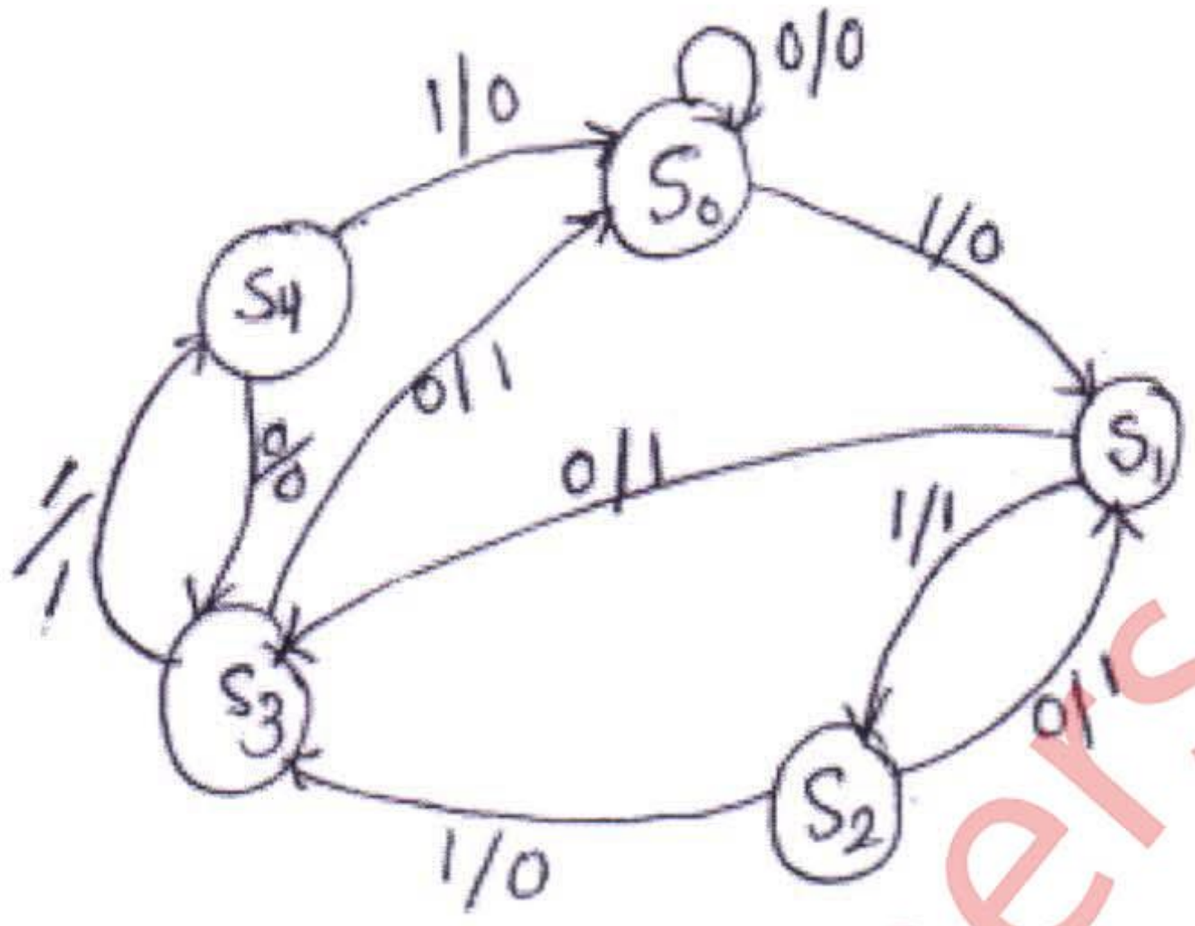

Figure 2

3. (a) Draw state diagram for BCD counter. Write a VHDL code for this state machine. **10**
   (b) Write a VHDL code for shift register. Use "Generic" and attributes in the code. List all the attributes used. **10**

4. (a) Using Data / controller partioning method. Draw ASM charts for bit counting circuit and explain it. **10**
   (b) Using WITH / SELECT / WHEN write a VHDL code for 8 : 1 multiplexer. **10**

5. (a) Explain in detail the structure of SRAM based FPGA. **10**
   (b) Write VHDL code for 4 bit carry look ahead adder. **10**

6. Write short notes on any **three** of the following :— **20**
   (a) RTL Simulation
   (b) Data Types in VHDL
   (c) State Reduction Techniques
   (d) ARRAYS in VHDL.
