ME ELX / SEM-II / CBCGS / MSVD / DT- 07-12-17

Q. P. Code: 27597

Duration: 3 Hours

Marks: 80

Note: (1) Question No.1 is compulsory.
(2) Attempt any three out of remaining.
(3) Assume suitable data wherever required.

Q.1(a)	Explain application of PLL in integrated circuit	5
(b)	Explain the necessity of guard ring in mixed signal environment	5
(c)	Draw and explain F-N model in detail	5
(d)	Explain the concept of VCO in detail	5
Q.2 (a)	Explain the concept of floor planning during mixed signal layout design in detail	10
Q.2(b)	Explain the concept of CMOS analog multiplier with detailed appropriate diagram.	10
Q.3 (a)	Explain Read write and erase operation of Floating gate memory	10
Q.3(b)	Explain non-ideal effects in PLL	10
Q.4(a)	Explain working of Schmitt trigger using CMOS	10
Q4 (b)	Explain Charge pump PLL.	10
Q.5(a)	Draw schematic of 6T SRAM cell and explain its stability criteria Also draw and discuss its butterfly diagram	10
Q.5(b)	A DAC has full scale voltage of 4.97 using 5V reference and its minimum output voltage is limited by the value of one LSB . Determine the resolution and dynamic range of converter.	10
Q.6	Write a short notes on (1) Speed consideration with respect to MOSFET as switch (2) Ring Oscillator (3) Sense Amplifier (4) Mixed signal layout issues	20

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